# ANALYSIS AND MODELING OF NONLOCAL AND DYNAMIC FLOATING-BODY EFFECTS FOR APPLICATION IN SCALED SOI CMOS TECHNOLOGY

By

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# ANALYSIS AND MODELING OF NONLOCAL AND DYNAMIC FLOATING-BODY EFFECTS FOR APPLICATION IN SCALED SOI/CMOS TECHNOLOGY

By

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This dissertation focuses on modeling, and its application thereof, of effects that are important in scaled silicon-on-insulator (SOI) CMOS devices. The first part of the dissertation concerns modeling of non-local effects such as velocity overshoot and impact ionization. The basis for the non-local modeling here is the simplified energy-balance (EB) equation. The EB equation keeps track of the carrier kinetic energy, or equivalently the carrier temperature, given the local electric field, and hence physically accounts for the temperature lagging the field. A "quasi-steady-state" approximation of the EB equation is used to transform the field-dependent mobility and ionization rate to their equivalent non-local counterparts. The transformed mobility is then used to model carrier velocity overshoot, while the temperature-dependent ionization rate is used to evaluate the non-local multiplication factor (defined as the integrated ionization rate). As a precursor to the velocity overshoot analysis/modeling, a comprehensive study of velocity saturation on the current drive of SOI MOSFETs is carried out.

The second part deals with effects inherent in the SOI technology due to the floating body. It is shown that in highly scaled fully depleted (FD) devices, an impact ionization-driven subthreshold kink can occur. The physical origin of this kink is explained, and is attributed to the back-surface of the SOI film being only mildly depleted. The meaning of FD/SOI is hence qualified. In certain transients, independent of impact ionization, the parasitic bipolar transistor is known to be activated in SOI MOSFETs due to dynamic body charging. A comprehensive quasi-2D BiMOS model for the bipolar transistor, including the (transient) transport current and the associated charges, is developed and implemented in SOISPICE. The modeling is based on the standard integral charge-control relationship, but is modified extensively to account for the gate-dependent hole density along the vertical direction (variable Gummel number), which can be important in certain applications. A novel design concept to suppress the bipolar effect, which is to enhance the diffusion capacitance, is presented.

For systematic model verification, as well as reliable evaluation of model parameters for a given technology, a physics-based parameter-evaluation methodology is outlined in the final part of the dissertation. This algorithm relies on the physical modeling in SOISPICE, and is hence relatively straightforward. It is shown that the model parameters evaluated from this process can provide insight into technology due to their physical nature. The utility of this algorithm is demonstrated by application to actual scaled SOI CMOS technologies.

# CHAPTER 1
# INTRODUCTION

The evolution of the integrated circuit (IC) industry over the past 25 years from large-scale integrated circuits (LSI) to present day ultra large-scale integrated circuits (ULSI) has been truly phenomenal [Dav95]. The primary driver for this growth has been the constant need for high-performance systems at reduced cost/benefit-per-function for the end user [Sem94]. Complementary metal-oxide-semiconductor (CMOS) has been the unanimous technology of choice for realizing these high-performance systems. In order to meet improved performance specifications, CMOS technology has been, and continues to be, scaled. The rules of scaling, which involve shrinking critical dimensions of the basic MOSFET, were first proposed by Dennard et al. [Den72], and later extended by Brews et. al. [Bre80]. Upon implementation, these rules have been more or less in accord with Moore's law [Moo75], which predicts the number of transistors/chip to roughly double every year. These scaling laws, however, are not ideal. The concept of ideal scaling, which involves maintaining constant electric fields in the MOSFET, while useful, has not been popular due to reluctance to depart from standardized voltage levels [Dav95]. Consequently, the trend of scaling to yield high-performance systems has been one where the supply voltage is hardly, or very slowly scaled.

Recently a new shift in the paradigm is taking place in the information industry, which will allow and demand faster scaling of the supply voltage [Dav95]. The main forces behind this change are the ability to produce complex systems in a chip, combined with the projected explosion in demand for portable and wireless systems which have very low power budgets. The scaling scenario for these low-voltage/low-power systems, as can be expected, is closer to the constant-electric field scaling theory [Dav95]. Consequently, two classes of systems, one focusing on high performance where speed is of utmost importance, and the other on low power, or significantly minimizing power consumption, will dominate CMOS technology.

Bulk-silicon MOSFETs have been the primary building block of CMOS technology to realize the goal of high-performance systems [Dav95]. However, it has been realized for a while now that there are serious limitations associated with its continued scaling for application to both the above mentioned classes of systems. For example, the tradeoffs amongst performance, leakage, and reliability becomes increasingly constrictive [Sem94]. An additional factor of concern is their increased susceptibility to alpha particle-induced soft errors [Dav95]. Silicon-on-insulator (SOI) CMOS technology has been purported to offer many advantages over its bulk counterpart. The benefits of a near-ideal subthreshold slope and enhanced current drive of fully depleted (FD) SOI MOSFETs, and the reduced junction capacitances of both FD and partially depleted (PD) MOSFETs, have been commonly cited in the literature [Sem94, Hu93]. Further, due to its reduced junction areas, it has been thought that SOI offers increased immunity to soft errors [Dav95]. The roadmap of the semiconductor industry association [Sem94] has in fact projected that CMOS on SOI may have to be used for highly scaled technologies of 0.1μm and below.

However, while SOI CMOS technology does have some of the above mentioned benefits, they may not all necessarily manifest in their entirety in scaled devices. Recent work [Yeh93] has shown that when the channel length of the FD/SOI is scaled, 2-D field fringing in the buried oxide can degrade its near-ideal subthreshold slope. Scaling the channel length of the FD/SOI MOSFET can also limit the enhancement in the saturation current drive compared to its bulk (and PD/SOI) counterparts [Fos93]. The PD/SOI MOSFET, which can be patterned after a bulk MOSFET, exhibits dynamic and hysteretic floating-body effects [Suh94b]. In addition to the above, both FD/ and PD/SOI MOSFETs also suffer from premature breakdown due to the activation of the parasitic bipolar junction transistor (BJT) in the floating body [You88, Cho91] by impact ionization near the drain. Further, it has been also pointed out [Pel95] that a low-voltage transient can activate the parasitic bipolar, independent of impact ionization.This transient bipolar effect is also known to decrease immunity to single-event upsets [Tos95].

To better understand, and possibly control the above effects, physical device models are necessary. Also, for application in device/circuit design in SOISPICE [Fos95], the models need to be compact. Some of the above mentioned effects have been comprehensively studied and accounted for in SOISPICE. For example, a physical 2-D model for fringing in FD/SOI [Yeh95] was developed, and applied to scaled FD/SOI MOSFETs for control of off-state leakage. Also, a comprehensive model for the non-fully depleted (NFD) a.k.a PD SOI MOSFET was recently developed [Suh95], and extensively used to study some of the dynamic and hysteretic floating-body effects.

Other effects that can be important in scaled SOI MOSFETs either have not been modeled previously, or have been accounted for in a non-physical manner. When the channel length is scaled, first carrier velocity saturation controls the drive current. In fact, this mechanism can limit the enhancement in current drive of FD/SOI MOSFETs. However, in very short channel devices, velocity overshoot [Sai88] which results due to carrier energy (or temperature) lagging the field, can possibly ameliorate the effects of velocity saturation. Hence, velocity overshoot which is inherently a nonlocal phenomenon, has to be accounted for in scaled devices. Also, conventional modeling of impact ionization assumes that the ionization rate is a function of the local field. This can not only result in pessimistic prediction [Cho90], but can also lead to incorrect dependences of the multiplication factor (defined as the integral of the ionization rate) on device structure, e.g., on the silicon film thickness. Therefore, impact ionization, which drives the bipolar-induced breakdown and kinks, has to be modeled as a non-local phenomenon wherein the ionization rate depends on the carrier temperature. An effect of velocity overshoot in scaled devices, which is to decrease the ionization rate, must also be considered.

As SOI MOSFETs are scaled, previously unacknowledged floating-body effects are becoming important. For example, when the FD/SOI MOSFET is designed to reduce 2-D fringing, e.g., by increasing body doping, unwanted floating-body effects can possibly be introduced. A subthreshold kink driven by impact ionization can occur in highly scaled FD/SOI MOSFETs. The kink, which is not well recognized, can increase the off-state leakage. Also, it is fundamentally different from the PD/SOI kink. New tradeoffs, as implied by this kink and 2-D fringing, will thus have to be accounted for in the design of FD/SOI MOSFETs.

Another floating-body effect, which was recently pointed out, is the significance of the transient bipolar effect in the SOI MOSFET [Pel95]. This low-voltage transient effect which is activated by dynamic body charging, can possibly cause upsets in DRAM cells [Suh96], and decrease the immunity to SEU [Tos95]. The existing model in SOISPICE [Fos95] is not adequate to comprehensively account for the parasitic BJT transport current and stored charges (which model the transient dynamics). A physical BiMOS model is necessary to account for the transient bipolar effect and to reliably assess its impacts at the device and circuit levels. Empirical sub-circuit representations consisting of separate bipolar and MOSFET models will be inadequate, and further, their parameter extraction would be tedious (due to two sets of model parameters).

An issue that is of great importance in reliable use of SOISPICE is parameter evaluation. A physics-based approach, wherein the (mostly physical or structure-dependent) model parameters can be evaluated by a systematic process, given the I-V characteristics, is therefore needed. Such a methodology will also help in model verification, as well as in identifying deficiencies. Extension of this methodology to calibrate the BiMOS model, e.g., the transient bipolar effect, must also be considered.

This dissertation, then, concerns with developing models in SOISPICE for non-local and dynamic floating-body effects that are important in scaled SOI CMOS technology, and subsequently applying it to design.

In the first part of Chapter 2, as a precursor to modeling velocity overshoot, the effect of velocity saturation on the current drive enhancement in SOI MOSFETs is studied. The study indicates that velocity saturation can limit the enhancement in current drive of scaled FD/SOI MOSFETs over its bulk (and PD/SOI) counterparts. This study does not include the effect of overshoot.

The second part discusses the development of a physical model for overshoot based on a simplified form of the energy balance (EB) equation. A quasi-steady state approximation of the EB equation is used to transform the field-dependent mobility into a temperature-dependent one. The concept of effective saturated drift velocity is next developed to make the model formalism consistent with the existing charge-based formalism in SOISPICE. The model predicts velocities that are in accord with data from literature. Velocity overshoot is shown to be significant in increasing the drive current (and reducing propagation delays) for channel lengths less than 0.15 μm.

In Chapter 3, a non-local model for impact-ionization current in SOI MOSFETs is presented. The basis for this modeling is once again the EB equation. Here a quasi-steady-state approximation of the EB equation is used to relate the field-dependent (Chynoweth) ionization rate to a temperature dependent one. The model is applied to the FD/ and the PD/SOI MOSFETs in all regions of operation. The model also accounts for the presence of impact ionization in the LDD and drain. Its "post-processing" implementation in SOISPICE is also discussed.

The model is then comprehensively verified via predictions of breakdowns and kinks in a variety of FD/ and PD/SOI devices. It is also applied to gain insight into optimal device/circuit design. The effect of velocity overshoot on impact ionization is also considered.

Chapter 4 first explains how subthreshold kinks can occur in highly scaled FD/SOI devices. The kink is distinguished from its PD counterpart, based on the underlying physics. This helps qualify the meaning of FD/SOI. A simple model to study the effect of this kink is then developed. The simulations suggest that designing conventional FD/SOI may be harder than previously thought, due to 2-D fringing and the kink.

Chapter 5 presents a comprehensive model for the parasitic bipolar transistor coupled to the SOI MOSFET. A quasi-2D BiMOS model for carrier injection, and its subsequent transport is characterized from a modified integral charge-control relationship. The associated stored charges are modeled consistently. The model also accounts for the gate-dependence of the hole density which can affect the gain of the (position-dependent Gummel number) BJT. The developed BiMOS model consists of one single set of parameters for the coupled BJT and MOSFET.

The model in SOISPICE is then thoroughly verified with 2-D MEDICI simulations, and also from device data. The model reveals the significance of the diffusion capacitance (due to stored charge) in addition to recombination. Insight gained from the modeling is used to then propose a novel concept to suppress the peak transient bipolar current via enhancing the diffusion capacitance.

In Chapter 6, a systematic, physics-based parameter evaluation methodology for the FD/ and PD/SOI models in SOISPICE, based on DC I-V characteristics is developed. The methodology is based on evaluating certain key physical (and structural) parameters from knowledge of device physics in a given region. The procedure, which avoids regions of self-heating, is then applied to actual FD/ and PD/SOI technologies and is shown to be a reliable approach to evaluation. This process is also shown to shed insight into technology, as the evaluated parameters can be correlated to process. The process is then extended to transients, where a transient (bipolar) measurement is used to calibrate some of the parameters.

Chapter 7 summarizes the work done in this dissertation, and also suggests guidelines for future research beyond this work.

Appendix A presents the derivation of the simplified EB equation, from the second moment of the Boltzmann transport equation (BTE). This equation is the basis for the non-local modeling of velocity overshoot and impact ionization in Chapters 2 and 3.

Appendix B gives the derivation of the electric field in the high-field portion of a weakly inverted channel for both FD/ and PD/SOI MOSFETs. These fields are used in Chapter 3 for evaluating the carrier temperature, and subsequently the impact-ionization multiplication factor.

# CHAPTER 2
# A STUDY OF CARRIER VELOCITY SATURATION AND OVERSHOOT IN DEEP-SUBMICRON SOI MOSFETs

## 2.1 Introduction

FD/SOI MOSFETs offer several potential advantages over their bulk-silicon counterparts for ULSI CMOS applications [Col91]. One of the advantages that has been widely noted is the enhanced current drive capability of the fully depleted device [Col91, Stu88, Lim84a], which is due mainly to the suppression of the body charge and transverse electric field that must be supported by the gate bias at the expense of inversion charge. This suppression tends to increase the drain saturation voltage and hence the saturation current, as well as the transconductance of the device. The same mechanism is responsible for the near-ideal subthreshold gate-voltage swing that is characteristic of the fully depleted SOI MOSFET [Col91]. However, as channel lengths are scaled aggressively, the effects of velocity saturation can negate some of this enhancement. Hence, any study focusing on performance enhancement of FD/SOI MOSFETs must consider thoroughly the effect of velocity saturation.

The first part of this chapter, then, describes a study of the effect of carrier velocity saturation on the saturation current $I_{DS(sat)}$ in deep-submicron SOI MOSFETs. The study, with SOISPICE confirmed by measurements, shows how velocity saturation in very short channel-length devices (due to scaling) can limit the enhancement in $I_{DS(sat)}$ of fully depleted (FD) SOI MOSFETs over those of its bulk and partially depleted (PD) counterparts.

An effect that can possibly alleviate this limitation is carrier velocity overshoot, which can obtain differently in FD and bulk MOSFETs. To assess the importance of velocity overshoot in scaled SOI MOSFETs, we have developed an analytical model based on a simplified version of the energy-balance equation. The second part of this chapter, then, focuses on modeling velocity overshoot, and applying the model in SOISPICE to study its potential benefits in scaled SOI MOSFETs.

## 2.2 Effects of Velocity Saturation on the Current Drive of SOI MOSFETs

### 2.2.1 Analysis

Most of the previous analyses of the current enhancement have focused on devices with relatively long channel lengths, and have ignored the effects of carrier drift velocity saturation on channel current. Yamaguchi, et al. [Yam89] did present experimental data reflecting how electron velocity saturation tends to reduce the relative current enhancement as the channel length is scaled to 0.7 μm, but they provided little insight concerning shorter devices. Here we emphasize deep-submicron devices, and show that the velocity saturation driven by high longitudinal electric field is effective in negating the current/transconductance enhancement in the fully depleted SOI MOSFET relative to the bulk-silicon device as the channel length is scaled toward 0.1 μm. The underlying analysis uses a physical model for the SOI MOSFET [Vee88a] implemented in SOISPICE-1 [Fit89]. The model gives good analytical insight, and simulations yield a performance benchmark of the fully depleted device relative to the bulk MOSFET for channel lengths ranging from 1.0 μm down to 0.1 μm. Measurements of fully depleted and non-fully depleted SOI MOSFETs, the latter of which emulates the bulk device, support the conclusion that the current drive enhancement is limited severely by the velocity saturation, although drain-induced effects, which also depend on the body charge condition, tend to obscure the limitation.

To put the analysis in proper perspective, we show in Fig. 2.1 results of DC SOISPICE-1 simulations that reflect the enhanced current drive capability of the fully depleted (FD) n-channel SOI MOSFET with relatively long channel length (L = 1 μm). The basis for SOISPICE-1 is our previously developed physical model [Vee88a] for the SOI MOSFET, which allows for two modes of operation: fully depleted body with the back surface depleted (FD), which is a mode of interest for ULSI CMOS, and fully depleted body with the back surface accumulated (TFA), which we use to model the bulk MOSFET. Indeed when the film thickness $t_b$ is set to the characteristic maximum depletion region width, $x_{d(max)}$, the TFA model approximates the bulk device well [Cho90] by matching the respective body capacitances (assumed to be constant along the channel). For the TFA (bulk MOSFET) simulation of Fig. 2.1, the body doping was $10^{17}$ $cm^{-3}$, which defines $x_{d(max)} \approx t_b = 100$ nm. For the FD simulation, the doping was $2 \times 10^{16}$ $cm^{-3}$ and $t_b = 100$ nm. For both devices, the front- and back-gate oxide thicknesses were 15 nm and 400 nm, respectively. To emphasize the effect of the body charge limitation on current, the (low-field) electron mobility was assigned the same value (700 $cm^2/V$-s) for both devices, and the same effective gate bias, $(V_{GfS} - V_{Tf}) = 1.7$ V, was used; the threshold voltage $V_{Tf}$ of each device was extracted from the simulated linear-region characteristics.

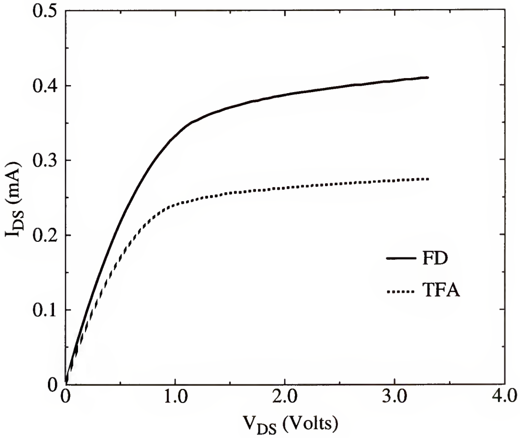


Fig. 2.1 SOISPICE-1-simulated current voltage characteristics of a fully depleted (FD) and a bulk (TFA) n-channel SOI MOSFET with 1-μm channel lengths. For both devices ($V_{GfS}$ - $V_{Tf}$) = 1.7 V, and the same low-field electron mobility (700 $cm^2$/V-s) was assumed.

The predicted saturation current of the FD (fully depleted) device in Fig. 2.1 is about 50% higher than that of the TFA (bulk) device. Whereas this difference is due predominantly to the more efficient $V_{GfS}$ control of channel charge in the FD device because of the suppressed charge and transverse field in the body, it is influenced by drain-induced effects such as DICE (drain-induced conductivity enhancement) and channel-length modulation [Vee88a], both of which yield increasing current with increasing $V_{DS}$. To gain insight concerning the current enhancement, we extract from the model formalism [Vee88a] the following expression for drain current at the onset of saturation, ignoring DICE:

$$I_{DS(sat)} = \left(\frac{WC_{of}}{1+\alpha}\right)\frac{m(V_{GfS}-V_{Tf})^2 v_{sat}}{1+m(V_{GfS}-V_{Tf})/(1+\alpha)} \tag{2.1}$$

where $m \equiv \mu_{eff}/2Lv_{sat}$ with $\mu_{eff}$ being the effective electron mobility in the saturation region and $v_{sat}$ the saturated drift velocity; and $\alpha \equiv C_b/C_{of}$ or $C_bC_{ob}/C_{of}(C_b + C_{ob})$ for TFA (bulk) or FD, respectively, with $C_{of}$ and $C_{ob}$ being the front- and back-gate oxide capacitances and $C_b = \varepsilon_s/t_b$ being the body (depletion) capacitance. The focus of previous commentary on the drive current enhancement [Col91, Stu88, Lim84a] is on the $1/(1 + \alpha)$ proportionality of $I_{DS(sat)}$ in (2.1). Obviously $\alpha$ for the FD device is smaller than that for the bulk device, which underlies the current enhancement. Physically, this inequality reflects the restricted depletion charge in the FD device, or the smaller transverse electric field, which implies, via Gauss's law, larger channel charge (and in fact higher $\mu_{eff}$ as well) for the same terminal bias conditions.

As can be seen in (2.1), indeed for relatively long L the current enhancement obtains. However, for shorter L such that $m(V_{GfS} - V_{Tf})/(1 + \alpha)$ is comparable to or greater than unity, the enhancement is limited. The physical reason for this limitation is the significance of electron velocity saturation in controlling $I_{DS(sat)}$ without total pinch-off of the channel at the drain. For deep-submicron MOSFETs, $v_{sat}$ controls the saturation of the device, and in the limit of very short L,

$$I_{DS(sat))} \rightarrow WC_{of}v_{sat}(V_{GfS} - V_{Tf}) \tag{2.2}$$

with the dependence on $\alpha$ negated. In this case, $I_{DS(sat)}$ is governed exclusively by the longitudinal field rather than by the transverse field, the latter of which underlies the current enhancement in the longer-L FD device. Note from (2.2) that any benefit from higher $\mu_{eff}$ as well as low $\alpha$ in the fully depleted SOI MOSFET is lost as L is scaled.

### 2.2.2 Results and Discussion

To assess how readily the current enhancement is limited as L is scaled, we show in Fig. 2.2 the relative enhancement of $I_{DS(sat)}$, at $V_{DS}$ = 3.3 V, versus L as predicted by SOISPICE-1 for the previously defined FD ($\alpha \approx 0.01$) mode compared with the TFA ($\alpha \approx 0.45$) mode, but with DICE and channel-length modulation turned off. For all L, ranging from 1.0 μm to 0.1 μm, the simulations were done with ($V_{GfS}$ - $V_{Tf}$) = 1.7 V. The underlying silicon substrate, or back gate, was biased commensurately with the back surface charge condition: for the TFA device, $V_{GbS}$ = -10 V, and for the FD device, $V_{GbS}$ = 1.0 V. The body was left floating, but the impact-ionization current, which drives floating-body effects [Cho91], was turned off. Note in Fig. 2.2 that for L < 0.7 μm, the enhancement drops steadily as L is shortened, and that for L = 0.1 μm, it is virtually gone. Note, however, that the L dependence of this limitation depends on $V_{GfS}$ and $\mu_{eff}$ as shown by (2.1).

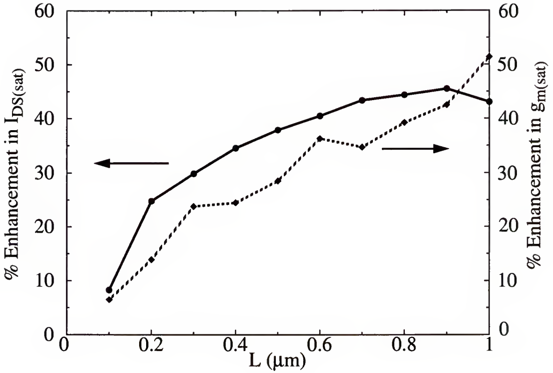


Fig. 2.2 Relative enhancement of $I_{DS(sat)}$ and $g_{m(sat)}$ versus L in the fully depleted MOSFET compared with the bulk device as predicted by SOISPICE-1. To stress the $\alpha$ effect in (2.1), DICE and channel-length modulation [Vee89] were turned off in the simulations, which were done at $V_{DS} = 3.3$ V and $(V_{GfS} - V_{Tf}) = 1.7$ V.

In fact the lower channel doping in the fully depleted SOI MOSFET suggests that $\mu_{eff}$ will be higher than in the bulk device, implying higher $I_{DS(sat)}$ for long L but meaning onset of the limitation at longer L. Note also, as discussed previously, that DICE and channel-length modulation [Vee89] tend to increase $I_{DS(sat)}$ and obscure the current-enhancement limitation caused by prevalent velocity saturation in the channel. These short-channel effects, however, are generally undesirable, and would be suppressed by proper scaling of the fully depleted device, e.g., of $t_b$ [Vee89], thereby revealing the limitation of the current drive enhancement in the deep-submicron device. The associated loss of the transconductance ($g_{m(sat)}$) enhancement for decreasing L as predicted by SOISPICE-1 is also shown in Fig. 2.2. We note that the minor fluctuations of the results plotted in Fig. 2.2 are probably due to numerical error stemming from the estimations of $V_{Tf}$. Indeed the relative enhancement of $I_{DS(sat)}$ gradually and monotonically approaches a maximum value as L increases above 1 µm, as implied by (2.1).

The limiting of the current enhancement in deep-submicron fully depleted SOI MOSFETs by carrier velocity saturation as predicted by SOISPICE-1 is confirmed by measurements of fully depleted (FD) and partially depleted (PD) n-channel devices. We compare in Fig. 2.3 measured saturated drain currents versus channel length for FD devices and PD counterparts, the latter of which are virtually bulk MOSFETs. The currents were measured at $V_{DS} = 3.3$ V with $(V_{GfS} - V_{Tf}) = 1.7$ V. The FD MOSFETs were fabricated (at Texas Instruments, Dallas, TX) in 120-nm SIMOX films with a $6 \times 10^{11}$ cm$^{-2}$ channel implant (boron) dose ($N_A \sim 2 \times 10^{16}$ cm$^{-3}$), and the PD MOSFETs in 300-nm films with a $4 \times 10^{12}$ cm$^{-2}$ (double-boron) dose ($N_A \sim 10^{17}$ cm$^{-3}$). The front

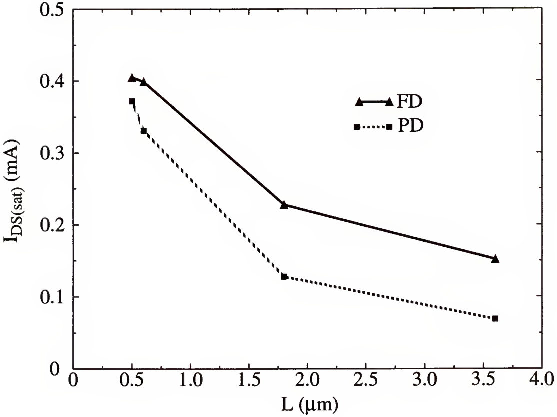


Fig. 2.3 Measured saturated drain current versus channel length for fully depleted (FD) n-channel SOI MOSFETs compared with that for partially depleted (PD $\cong$ bulk) counterparts; all devices have 2.4-μm gate widths. All data were taken at $V_{DS}$ = 3.3 V and ($V_{GfS}$ - $V_{Tf}$) = 1.7 V.

gate oxide thicknesses are 15 nm for the FD devices and 20 nm for the PD devices. All devices have 2.4-μm gate widths, and intrinsic body-source ties which disable floating-body effects. Note for the longer-L devices, the FD current is significantly higher than the PD current; at L = 1.8 μm the current enhancement is about 80%, which translates to 35% when the difference between the gate oxide thicknesses is factored out. Much of this enhancement is due to the $\alpha$ effect reflected by (2.1), but some of it is due to the higher electron mobility in the FD device resulting from the lower channel doping. Note however for decreasing submicron L, the FD $I_{DS(sat)}(L)$ variation shows a leveling, which indeed can be attributed to velocity saturation as we have discussed. This leveling is not obvious in the PD data, which is consistent with a higher electric-field onset for velocity saturation due to a lower $\mu_{eff}$. The comparative results in Fig. 2.3 thereby show a loss of the current drive enhancement of the FD device relative to the PD (bulk) counterpart for scaled L; at L = 0.5 μm, the enhancement has been limited to less than 10%. The associated measured transconductances versus L are compared in Fig. 2.4. Note that $g_{m(sat)}$ of the FD device actually decreases slightly with L in the submicron range. This is consistent with SIMOX device data presented in [Mik89], where a material-related explanation was suggested. The trends shown by these data agree with those predicted by SOISPICE-1 in Fig. 2.2. The measured loss of current enhancement is more severe because of the effects of DICE and channel-length modulation in the PD device, which tend to be ameliorated in the FD device [Vee89]. These effects were turned off in the SOISPICE-1 simulations.

We stress however that carrier velocity overshoot due to non-stationary effects in the deep-submicron device [Ant91] has not been taken into account in this study. Velocity

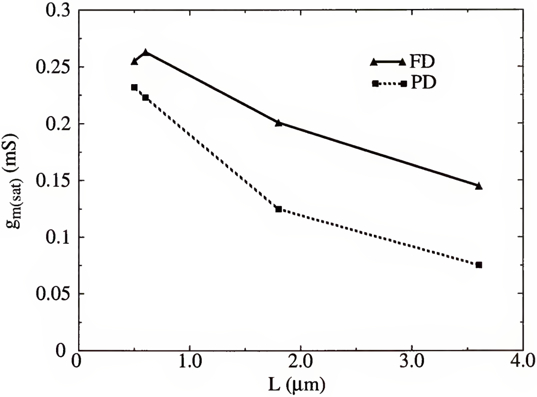


Fig. 2.4 Associated with Fig. 2.3, measured saturation-region transconductance versus channel length for the fully depleted (FD) device compared with the partially depleted (PD ≅ bulk) device.

overshoot, due to non-stationary effects could obtain differently in FD and PD devices, and hence ameliorate some of the loss in current enhancement of FD/SOI MOSFETs. In order to study the effects of overshoot in scaled SOI/CMOS devices and circuits, a compact model, is the focus of the following sections, is necessary.

## 2.3 Velocity Overshoot

One of the beneficial effects of scaling MOSFETs to the deep-submicron regime is the possibility of enhanced current drive due to the occurrence of velocity overshoot. The phenomenon of overshoot has been well understood for a while now [Ruc72, Hua77]. Carriers traversing in regions with large field gradients acquire energy at a finite rate implied by the non-zero energy relaxation time. Consequently, these carriers do not get as hot as implied by the local field and are hence free to overshoot the velocity implied by the steady-state velocity-field relationship. When overshoot occurs, the velocity at any given point does not depend on the local field, but rather on the carrier temperature at that point. For this reason, velocity overshoot is termed a "non-local" phenomenon.

Many rigorous analyses for overshoot have been done in scaled silicon MOSFETs based on Monte Carlo (MC) methods [Lau90] or on solving complex hydrodynamic and energy-transport equations [Bac85, Bor91]. While the MC method is the fundamentally physically correct approach, it is too computationally intensive. An alternate approach is to use the hydrodynamic method, and in fact a number of device simulation programs (e.g., MEDICI [Med94]) have started using them. While such an approach is computationally feasible for device simulation, it's efficacy in circuit simulation is questionable. A word of caution regarding using the hydrodynamic or energy-transport approach is that the results may not be completely unambiguous. For example, the various relaxation times are typically extracted from uniform-field MC simulations, and are hence imprinted with the uniform-field form of the distribution function [Bor91]. This can render the results of the simulations somewhat equivocal in devices with large field gradients.

### 2.3.1 Model Development

Previous approaches to analytical modeling of velocity overshoot have been based on the augmented drift-diffusion approach [Jin91, De93]. The validity of such an approach is questionable, as it is based on a length coefficient, which is phenomenological. On the contrary, the energy relaxation length, which is the critical transport parameter for hydrodynamic models, is based on a physically sound concept and has been well characterized over a wide range of carrier energies. For purposes of accounting for velocity overshoot in compact models, a reasonable approach is to use a simplified form of the energy-balance equation [Slo91] to describe the energy relaxation process:

$$\frac{d}{dy}(T_e(y) - T_L) + \frac{(T_e(y) - T_L)}{\lambda_e} = \frac{2qE_y(y)}{5k_B} \tag{2.3}$$

where $T_e(y)$ is the carrier temperature, $T_L$ is the lattice temperature, $\lambda_e$ is the energy relaxation length, $E_y(y)$ is the longitudinal electric field. (For a detailed derivation of (2.3) from the second moment of the energy balance equation, please see Appendix A.) The first term in (2.3) physically accounts for the fact that the carrier temperature lags the local electric field. Use of local-field models is equivalent to neglect of this term. The solution to (2.3) is given by

$$T_e(y) - T_0 = \frac{2q}{5k}\int_0^y \exp\left[\frac{u-y}{\lambda_e}\right]|E(u)|du + C\exp\left(-\frac{y}{\lambda_e}\right) \tag{2.4}$$

where C is an integration constant dependent on $T_e(0)$. Equation (2.3) will be first used to transform the field-dependent mobility into a (carrier) temperature-dependent one. Subsequently, (2.4) will then be used to characterize the temperature (and the non-local velocity) in the channel of the MOSFET. (Note that even though the model developed here is for application in SOI MOSFETs, it can be extended to bulk MOSFETs in a straightforward manner.)

Traditional device modeling of carrier transport based on the drift-diffusion approach relies on velocity-field relationships, extracted from measurements under *homogeneous* conditions [Sod84], such as

$$v(E) = \left(\frac{\mu_{eff}}{\left(1 + \left(\frac{\mu_{eff}E_y}{v_{sat}}\right)^2\right)^{\frac{1}{2}}}\right)E_y \tag{2.5}$$

where $\mu_{eff}$ is the low-field mobility that accounts for surface and impurity scattering and is also a function of the transverse electric field in the channel. This model is valid as long as the field is quasi-homogenous. In scaled MOSFETs, the carrier temperature lags the local electric field, even in the channel of the device, resulting in velocity overshoot.

To obtain an expression for non-local velocity, we first apply (2.3) under uniform, or steady-state conditions ($dT_e/dy = 0$), which gives $(T_e - T_L) = 2/5q/kE_y\lambda_e$. This steady-state $T_e$-E relationship is used to transform the field-dependent velocity in (2.5) into a temperature-dependent one,

$$v(T_e(y)) = \left( \frac{\mu_{eff}}{\left(1 + \left(\frac{\mu_{eff}(T_e(y) - T_L)}{v_{sat}A}\right)^2\right)^{\frac{1}{2}}} \right) E_y(y) \tag{2.6}$$

where $A = 2/5q/k\lambda_e$. Now, in an actual device where the field in the channel is not homogeneous, $T_e(y)$ is given by (2.4), and the carrier velocity thus obtained from (2.6) is non-local. Equation (2.6) will be used to develop the concept of an *effective* saturated drift velocity $v_{sat(eff)}$, that defines the onset of current saturation, subject to overshoot. This will be the topic of discussion in the next section.

#### 2.3.1.1 Concept of Effective Saturated Drift Velocity

Even though (2.6) properly accounts for velocity overshoot, its spatial form is not conducive for use in compact models. For instance, standard integration of velocity to obtain the current as in [Vee88b] is very cumbersome with the velocity model in (2.6). However, we can simplify the model formalism by defining from (2.6) a spatially independent, *effective* saturated drift velocity. The concept of $v_{sat(eff)}$ takes advantage of the fact that in a scaled MOSFET the channel current always tends to saturate due to carrier scattering (e.g., with optical phonons) as the drain bias is increased. Mathematically, the onset of current saturation implied by (2.5) and (2.6) is defined by the fact that the denominator (which models scattering) becomes much greater than one. However, in (2.6) this onset is dependent on carrier temperature, rather than the field. Use of $v_{sat(eff)} > v_{sat}$ will delay the onset of saturation, and increase the drain saturation voltage $V_{DS(SAT)}$ for scaled devices, which is precisely what velocity overshoot does. Hence, we define $v_{sat(eff)}$ from (2.6) to be the velocity at the drain ($y = L$) when $V_{DS} = V_{DS(SAT)}$. This condition for *onset* of current saturation can be expressed as

$$v_{sat(eff)} \equiv v(T_e(L)) = \frac{\mu_{eff} E_y(L)}{D} \tag{2.7}$$

where $E_y(L)$ and $T_e(L)$ are the field and the corresponding carrier temperature at the onset of current saturation, and D is a constant that is larger than 1, and typically lies between 3 and 5. Note that the saturated velocity now is a spatially-independent constant, but is dependent on the structure (e.g., L) as well as the bias conditions as implied by (2.7). The advantage of using this concept is that it will preserve the *form* of the existing charge-based SOI MOSFET models [Fos95] while accounting for overshoot in a physical manner.

With $v_{sat(eff)}$ in (2.7), we now redefine a spatial velocity along the channel as

$$v(y) = \left( \frac{\mu_{eff}}{\left(1 + \left(\frac{\mu_{eff} E_y}{2 v_{sat(eff)}}\right)\right)} \right) E_y \quad . \tag{2.8}$$

The above equation is similar to the model for carrier velocity in [Vee89] with the exception that the $v_{sat}$ is replaced by $v_{sat(eff)}$. To evaluate $v_{sat(eff)}$ we have to solve for the lateral field $E_y(y)$ and the carrier temperature $T_e(y)$ in the channel. The lateral field in the channel can be obtained by integrating the channel current from the strong-inversion model formalism [Vee89] between 0 and an arbitrary point y. The resulting field is expressed as

$$E_y(y) = \frac{E_y(0)}{(1 - by)^{\frac{1}{2}}} \quad , \tag{2.9}$$

where $E_y(0)$ is the lateral field at the source ($y = 0$) given by

$$E_y(0) = \frac{\left(Q_{cf}(0) - \frac{I_{DS(onset)}}{2v_{sat(eff)}}\right)}{2C_{of}(1+\alpha)} \quad , \qquad (2.10)$$

and b is defined as

$$b = \frac{8I_{CH}Wv_{sat(eff)}^2C_{of}(1+\alpha)}{\bar{\mu}_{eff}(2WQ_{cf}(0)v_{sat(eff)} - I_{DS(onset)})^2} \quad . \qquad (2.11)$$

In (2.10) and (2.11), $Q_{cf}(0)$ is the channel charge at $y = 0$, $I_{DS(onset)}$ is the channel current at the onset of saturation, $C_{of}$ is the front-oxide capacitance, and $\alpha$ is a coupling factor ($C_b/C_{of}$ for PD and $C_bC_{ob}/(C_{of}(C_b+C_{ob})$ for FD), W is the width of the device, and $\mu_{eff}$ is an effective mobility. The carrier temperature at L is obtained by using (2.9) in (2.4) as

$$T_e(L) - T_0 = \frac{2q}{5k}E_y(0)\exp\left(-\frac{L}{\lambda_e}\right)\int_0^L \frac{\exp\left[\frac{y}{\lambda_e}\right]}{(1-by)^{\frac{1}{2}}}dy \quad . \qquad (2.12)$$

Now, (2.6), (2.7) with D, (2.9), (2.10), (2.11), and (2.12) define $v_{sat(eff)}$ completely (but implicitly). Therefore, the system of equations (2.7), (2.9) and (2.12) is solved iteratively to obtain $v_{sat(eff)}$, and $I_{DS(onset)}$ by a simple bisection method. Note that since (2.12) can not be evaluated analytically, it is obtained by numerical (Romberg) integration.

#### 2.3.1.2 Channel Current

Once $v_{sat(eff)}$ is obtained, we follow the strong-inversion analysis in [Vee89] to express the channel current in the triode region as

$$I_{CH} = \frac{-W\bar{\mu}_{eff}[Q_{cf}^2(L) - Q_{cf}^2(0)]}{2LC_{of}(1+\alpha)\left(1 + \frac{\bar{\mu}_{eff}V_{DS}}{2v_{sat(eff)}L}\right)} \tag{2.13}$$

while the saturation current is given by

$$I_{CH} = -WQ_{cf}(L_e)v_{sat(eff)} \quad . \tag{2.14}$$

The channel-length modulation analysis (that describes $L_e$) is similar to [Vee88a], but with $v_{sat}$ replaced by $v_{sat(eff)}$.

### 2.3.2 Model Implementation/Verification

The model was implemented in SOISPICE to assess the benefits of overshoot in scaled SOI/CMOS technologies. As mentioned earlier the process of defining $v_{sat(eff)}$ required the use of a bisection method to solve for the system of equations (2.9)-(2.12). Basically these equations are used to first define the drain voltage $V_{DS(sat)}$ for onset of current saturation with velocity overshoot. Subsequent analyses for the current and channel-length modulation [Vee88a] is done consistently by replacing $v_{sat}$ with $v_{sat(eff)}$ everywhere.

The overshoot model predicts velocities in scaled devices that are in good agreement with published data. For example, the predicted *average* electron velocity ($<v> \equiv g_m/(WC_{of})$) versus channel length and low-field mobility for a fully depleted (FD) SOI MOSFET in Fig. 2.5 is in accord with the measurements of [Ass93] and the numerical simulations of [Pin93]. Note that the average velocity for typical mobilities exceeds $v_{sat}$ for L <

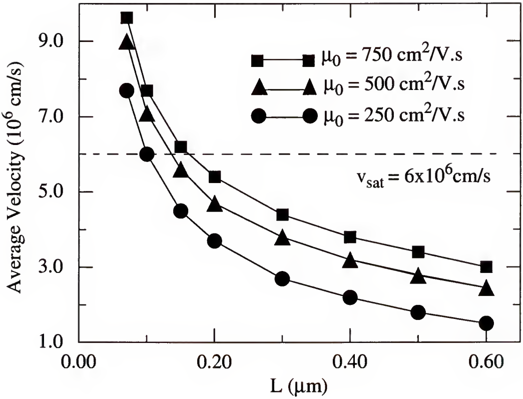


Fig. 2.5 Model-predicted average carrier velocity in a fully depleted SOI MOSFET; $t_b$ = 30 nm, $t_{of}$ = 9nm.

0.15 μm, indicating that velocity overshoots significantly in the channel. (The value of $v_{sat}$ used in all the simulations here was $6x10^6$ cm/s, based on the experimental results of [Ass93].)

### 2.3.3 Results and Discussion

The model predictions in Fig. 2.6 show how overshoot affects saturation current. Firstly, for relatively long L and low gate bias, $I_{DS(sat)}$ is controlled predominantly by pinch-off at the drain. The reason for pinch-off controlling saturation current for these cases is because the drain bias required for pinch-off ($V_{DS(sat)\_PO} \approx (V_{GfS}-V_{Tf})/(1+\alpha)$) is smaller than that required for carrier velocity saturation. Any further increase in the drain bias beyond $V_{DS(sat)}$, will only affect the velocity and field distribution near the drain (to maintain current continuity). The average velocity will not be affected. As L is scaled $I_{DS(sat)}$ is controlled by velocity saturation since $V_{DS(sat)} < V_{DS(sat)\_PO}$. Consequently, the ratio of the saturation current $I_{DS(sat)}$ to the pinch-off current $I_{PO}$ ($\propto$ vsat(eff)/ ($\mu_{eff}$*$V_{DS(sat)\_PO}$/L)) decreases as L is scaled down. However, velocity overshoot does help in enhancing the current, as shown by the solid curves, especially for deep-submicron L.

Secondly, as the gate bias is increased, the current is limited by velocity saturation even for long L because the drain bias to cause pinch-off $V_{DS(sat)\_PO}$ increases correspondingly; hence the enhancement due to overshoot is evident even for longer L compared to the case of the low gate bias. An interesting insight from (2.6) is that the cross-over of the limiting current due to velocity saturation ($WC_{of}(V_{GfS}-V_{Tf})v_{sat}$) and the actual $I_{DS(sat)}$ is an exact signature of overshoot-controlled behavior [Sai88] in a scaled device.

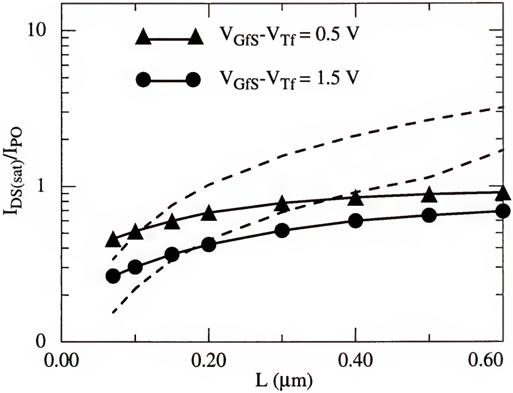


Fig. 2.6 Model-predicted ratio (log scale) of saturated current (with overshoot) to pinch-off-limited current, $I_{PO}$; the dashed curves represent ratios of the maximum possible $I_{DS(sat)}$ without overshoot $\{WC_{of}(V_{GfS}-V_{Tf})v_{sat}\}$ to $I_{PO}$ for the same $V_{GfS}$ noted.

In fact after this cross-over, the velocity would be greater than $v_{sat}$ everywhere in the channel. Further, the simulations suggest due to the higher low-field mobility, velocity overshoot will be more significant in FD than its bulk (or PD) counterpart as indicated in Fig. 2.5. Consequently, some of the limitation in enhancement in the current drive for the FD device will be ameliorated. A device design to exploit overshoot in PD is to use a super-steep retrograde [Ant91] where the doping in the surface would be small enough to increase the low-field mobility, and consequently, velocity overshoot as implied by Fig. 2.5. The current enhancement due to the velocity overshoot implies significant speed improvement in deep-submicron SOI CMOS. Predictions of gate propagation delay derived from SOISPICE simulations of a three-stage unloaded inverter circuit are plotted in Fig. 2.7 versus L. Comparison of this delay with that predicted without overshoot reveals the speed benefit of (electron) velocity overshoot when L<0.15 μm.

### 2.3.4 Effect of Overshoot on Impact Ionization

Another benefit of overshoot, unique to SOI MOSFETs, is its effect on impact ionization. Impact ionization drives parasitic BJT-induced drain-source breakdown. However, for very short L overshoot can increase the drain saturation voltage and decrease the maximum field (and carrier temperature). Consequently, the non-local impact-ionization multiplication factor, ((M-1), whose modeling will be discussed extensively in the next chapter, can significantly decrease due to overshoot in scaled devices as shown in Fig. 2.8. This can also significantly improve breakdown voltage, as will be discussed in the next chapter.

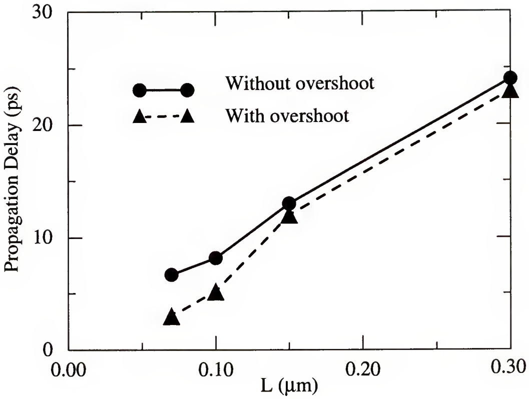


Fig. 2.7 SOISPICE-simulated propagation delay of a 3-stage unloaded SOI CMOS inverter; $V_{DD}$ = 1.5 V. Enhancement in speed is significant for L < 0.1 μm.

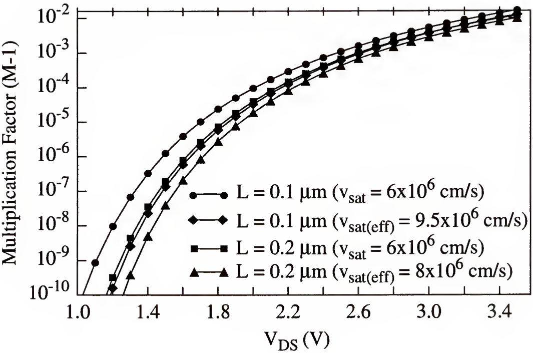


Fig. 2.8 Effect of velocity overshoot on multiplication factor, (M-1). As can be seen, (M-1) in the shorter channel-length (L = 0.1 µm) device decreases more due to greater overshoot.

## 2.4 Conclusions

Severe limitation of current-drive enhancement in deep-submicron fully depleted SOI MOSFETs has been reported based on SOISPICE-1 simulations supported by measurements of test devices and analytical insight. The theoretical/experimental analysis showed that carrier drift velocity saturation in the short-channel device effectively negates the current enhancement resulting from the suppressed transverse electric field and body charge in the fully depleted device. For L = 0.1 μm, the enhancement is virtually eliminated. The associated superior transconductance of the fully depleted SOI MOSFET relative to its bulk counterpart is lost as well. It must be stressed that this study however, did not include the effect of velocity overshoot.

As shown in the second part of this chapter, overshoot does ameliorate the loss of enhancement in saturation current. Indeed, for scaled L carrier velocity can overshoot everywhere in the channel. Further, overshoot also decreases the multiplication factor due to impact ionization, which increases the breakdown voltage. Non-local modeling of the multiplication factor due to impact ionization, and its effect on breakdown will be discussed in the following chapter.

# CHAPTER 3
# NON-LOCAL IMPACT IONIZATION IN SOI MOSFETs: MODELING, VERIFICATION, AND APPLICATION

## 3.1 Introduction

As SOI MOSFETs are aggressively scaled, premature breakdown and off-state latch, due to the parasitic BJT driven by impact ionization [Cho91], threaten their viability. Other floating-body effects driven by impact ionization, e.g., current kink effects [Suh95], are problematic as well. Reliable modeling of these effects requires a non-local characterization of impact-ionization current [Slo91], in contrast to conventional local-field models that tend to overestimate the carrier generation rate. Furthermore, to study the noted effects at the circuit level, the modeling has to be compact. In this chapter the needed model is described and developed, and further, is applied in the predictive circuit simulator SOISPICE [Fos95] to the optimal design of SOI CMOS devices and circuits, with emphasis on control of the DC BJT effects.

Conventional local-field analyses [Hu85, Cho90] of impact ionization assume that the carrier energy correlates directly with the local electric field, ignoring effects of energy relaxation. Consequently, these analyses not only overestimate the generation current, but they fail to account for its dependence on the device structure, e.g., on channel length. The most rigorous way to model non-local effects, as mentioned in the previous chapter, is by Monte Carlo approach. However, the computational burden associated with this approach does not allow for efficient device simulation. Another approach, which solves for the first three moments of the Boltzman transport equation, is the hydrodynamic model which is now included in many state-of-the-art device simulators (e.g., MEDICI [Med94]). It is intensive as well, and not useful for circuit simulation. A simple form of energy transport has been developed [Slo91, Ago92] for device simulation that characterizes the average carrier temperature from the electric-field distribution. Such an approach, which is implemented as post-processing, provides reasonable insight into the physics of energy transport.

This simplified non-local modeling, used in the previous chapter to model velocity overshoot, is used herein to characterize, for the first time, impact-ionization current in compact SOI MOSFET models for circuit simulation. The models, for fully depleted (FD) and partially depleted (PD) SOI CMOS, are implemented in SOISPICE [Fos95], and are verified via predictions of breakdown and kinks in test devices having different channel lengths, doping densities, and SOI film thicknesses. SOISPICE is used to gain insight regarding optimal device and circuit design tradeoffs involving the BJT breakdown. In particular, the efficacy of the LDD in scaled SOI CMOS is assessed.

## 3.2 Model Development

In compact SOI MOSFET models, the (weak) impact-ionization current can be expressed as [Cho91]

$$I_{Gi} = (M-1)(I_{CH} + I_{BJT}) \tag{3.1}$$

where (M-1) is the multiplication factor, $I_{CH}$ is the channel current, and $I_{BJT}$ is the transport current associated with the parasitic BJT. Our focus here is on new non-local modeling of (M-1) for both weak and strong inversion. In one dimension at a surface,

$$(M-1) \cong \int \alpha(T_e)dy \tag{3.2}$$

where $\alpha$ is the ionization rate. Physically, as pointed out earlier, the ionization rate is driven by the (average) carrier kinetic energy w, or equivalently the carrier (e.g., electron) temperature $T_e$, which can differ from the lattice temperature $T_0$. The key to the compact model development is the characterization of $T_e(y)$, based on the lateral field E(y). This, in principle, requires solving the energy-balance equation, which is non-trivial [Lun90]:

$$\frac{\partial w}{\partial t} + \dot{v} \bullet \nabla w = -q\dot{E} \bullet \dot{v} - \frac{k}{n}\nabla \bullet nT_e\dot{v} - \frac{1}{n}\nabla \bullet \kappa \nabla T_e - \frac{w - w_0}{\tau_w} \tag{3.3}$$

where $w \cong (3kT_e)/2$, $w_0 = (3kT_0)/2$, v and n are the electron velocity and concentration, E is the electric field, and $\kappa$ is the electron thermal conductivity. A simplified form of (3.3), which is (2.5) described in Chapter 2, in one dimension can be obtained if we first assume that velocity overshoot is insignificant, i.e., that carrier velocity is saturated in high-field regions, and that carrier diffusion is negligible. We repeat (2.5) here for the sake of convenience,

$$\frac{d}{dy}(T_e(y) - T_0) + \frac{(T_e(y) - T_0)}{\lambda_e} = \frac{2q|E(y)|}{5k} \tag{3.4}$$

where $\lambda_e$ is the energy-relaxation length. The solution to (3.4) approximates the electron temperature directly from the electric field distribution:

$$T_e(y) - T_0 = \frac{2q}{5k}\int_0^y \exp\left[\frac{u-y}{\lambda_e}\right]|E(u)|du + C\exp\left(-\frac{y}{\lambda_e}\right) \tag{3.5}$$

where C is a constant dependent on $T_e(0)$ for the region of interest. The first term in (3.4) physically accounts for the fact that the carrier temperature lags the local field. Use of local-field models is equivalent to neglect of this term.

With $T_e(y)$ in (3.5), a "quasi-steady-state" approximation is then used to transform the field-dependent (Chynoweth) ionization rate into a temperature-dependent one [Slo91]. This approximation yields

$$\alpha = \alpha_0 \exp\left(-\frac{\beta_0}{A(T_e - T_0)}\right) \tag{3.6}$$

where $A = 5k/(2q\lambda_e)$. With (3.2), (3.5), and (3.6), we can estimate (M-1) for both strong and weak inversion in the SOI MOSFET from knowledge of E(y) along the surface. The integration in (3.2) must cover the high-field region of the channel, the LDD if there is one, and the drain. We exemplify the analysis by detailing $I_{Gi}$ in FD/ and PD/SOI MOSFETs.

### 3.2.1 Strong-Inversion Analysis

Impact ionization in strong inversion in the SOI MOSFET triggers the BJT-defined source-drain breakdown of the device, as well as saturation-region current kinks. The analyses of impact ionization in this region for both the FD/ and PD/SOI MOSFET are very similar. The underlying multiplication factor is modeled as follows.

### 3.2.1.1 Channel Region

A quasi-2-D analysis [Vee88a] accounting for carrier velocity saturation yields E(y) $\cong E_c\cosh(y/l_c)$ in the modulated, high-field region of the channel; $E_c$ is the critical field for velocity saturation, $l_c = t_b(C_b\beta/(2C_{of}(1+\alpha)))^{1/2}$ is a characteristic length that reflects the field gradient in the high-field region, $t_b$ is the SOI film thickness, $C_b$ and $C_{of}$ are capacitances associated with the film and the front oxide, respectively. (The parameters $\alpha$ and $\beta$ have their usual definitions for the FD/ and the PD/SOI MOSFET [Vee88b, Suh95a].) Using this field in (3.5), we obtain in the modulated region of the channel ($0 < y < \Delta L$ in Fig. 3.1)

$$T_e(y) - T_0 \cong \frac{qE_c}{5k}\frac{\exp\left(\frac{y}{l_c}\right)}{\frac{1}{l_c}+\frac{1}{\lambda_e}} \quad . \tag{3.7}$$

In the derivation of (3.7) we assumed that $T_e(0) \cong T_0$, which although not exact does not undermine the accuracy of the subsequent expression for (M-1). Note that when $l_c >> \lambda_e$, the carrier temperature approaches its "steady-state" value ($T_0$ + E/A) corresponding to the local field. However, for ultra-thin films where $l_c < \lambda_e$, the carrier temperature never reaches its steady-state value, signifying the non-local nature of carrier transport in scaled devices.

The multiplication factor in (3.2) is rewritten as

$$(M-1) = \int \alpha(T_e)\frac{dT_e}{\left(\frac{dT_e}{dy}\right)} \quad . \tag{3.8}$$

Then using (3.6) and (3.7) in (3.8), we obtain

$$(M-1)^{Ch} = \int_0^{\Delta L} \alpha_0 l_c \exp\left(-\frac{\beta_0}{A(T_e - T_0)}\right)(T_e - T_0) d\left(-\frac{1}{(T_e - T_0)}\right) \quad . \quad (3.9)$$

Since the temperature increases monotonically as $y \rightarrow \Delta L$, we can obtain a good estimate for (3.9) by removing the term ($T_e$-$T_0$) from the integral, and then carrying out the integration:

$$(M-1)^{Ch} \cong \frac{\alpha_0 l_c A}{\beta_0}(T_e(\Delta L) - T_0)\exp\left(-\frac{\beta_0}{A(T_e(\Delta L) - T_0)}\right) \quad ; \quad (3.10)$$

$\Delta L$ is defined by the quasi-2-D analysis [Vee88a] as

$$\Delta L \cong l_c \ln\left(\frac{E_m}{E_c} + \sqrt{\left(\frac{E_m}{E_c}\right)^2 + 1}\right) \quad (3.11)$$

where $E_m = (V_{DS}\text{-}V_{DS(eff)})/l_c$ is the maximum field in the channel.

### 3.2.1.2 LDD

In scaled MOSFETs, an LDD is commonly used to reduce the maximum field in the channel, thereby reducing hot-carrier effects, including $I_{Gi}$. In the LDD, we first characterize the electric field using the 1-D Poisson equation with boundary conditions implied by the channel analysis [Vee88a]. The resulting possible field distributions in the LDD are shown in Fig. 3.1. The carrier temperature corresponding to the most general case (case b) is obtained by substituting in (3.5) $E = E_m - S\,(y - \Delta L)$ for $\Delta L \le y \le \Delta L + L_D$, where $S = qN_{LDD}/\varepsilon$ and $L_D$ is the (variable) width of the depletion region in the LDD, and $E = r_d I_{DS}$ for $\Delta L + L_D \le y \le \Delta L + L_{LDD}$, where $r_d = 1/(q\mu_{n(LDD)}N_{LDD}Wt_b)$ is the resistance of the

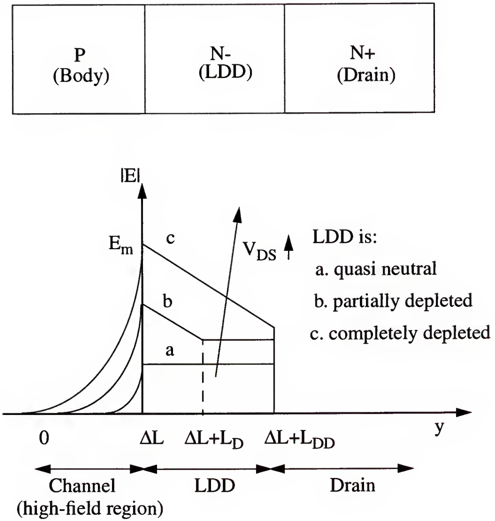


Fig. 3.1 Electric field distributions in the LDD; for increasing $V_{DS}$, the distributions a, b, and c obtain sequentially.

LDD per unit length and $I_{DS}$ is the (total) drain current. The corresponding (M-1) defined by (3.2) and (3.6) is evaluated numerically by Romberg integration.

### 3.2.1.3 Drain

In scaled devices, significant impact ionization can occur in the drain region, depending on the applied bias and the LDD length, even though the field in the drain is approximately zero. This is a result of the carrier temperature lagging the local electric field as illustrated by our model predictions in Fig. 3.2. The carrier temperature in the drain follows from (3.4), with E(y) = 0 and the boundary condition from the LDD analysis. The corresponding (M-1) in the drain is evaluated analytically with approximations similar to those used in the channel analysis.

The composite (M-1) is now given as the sum of the individual multiplication factors in the channel, the LDD, and the drain:

$$(M-1)^{\mathrm{Total}} = (M-1)^{\mathrm{Ch}} + (M-1)^{\mathrm{LDD}} + (M-1)^{\mathrm{Drain}} \quad . \qquad (3.12)$$

An interesting insight from Fig. 3.2 is that the peak ionization rate typically occurs in the LDD, and not in the drain end of the channel as is predicted by local-field models.

### 3.2.2 Weak-Inversion Analysis

Impact ionization in weak inversion triggers the BJT-defined off-state latch in the SOI MOSFET, as well as subthreshold current kinks. We first consider weak inversion in the FD device.

### 3.2.2.1 FD/SOI

Here carriers possibly flow at both the front and back surfaces of the silicon film [Yeh93]. Therefore, carrier multiplication can occur at both surfaces. A quasi-2D analysis similar to that in [Gre93], with boundary conditions consistent with transport in weak inversion, yields the field in the high-field region at the front and back surfaces, (Please see Appendix B for this derivation.)

$$|E_f(y)| \cong |E_b(y)| \cong \frac{\eta l_c^2}{l_{cf}} \sinh\left(\frac{y}{l_{cf}}\right) \qquad (3.13)$$

where $l_{cf}$ $(= l_{cb}) = t_b(C_b/(C_{of} + C_{ob}))^{1/2}$ is a weak-inversion characteristic length, and $\eta = 2V_{DS}/L^2$. The corresponding $T_e(y)$ can obtained by using (3.5) as

$$T_e^{Wk}(y) - T_0 \cong \frac{\frac{\eta l_c^2}{l_{cf}} q \exp\left(\frac{y}{l_{cf}}\right)}{5k \left(\frac{1}{l_{cf}} + \frac{1}{\lambda_e}\right)} \quad , \qquad (3.14)$$

while (M-1), which is estimated analytically at both surfaces, is given by,

$$(M-1)^{Wkf} \cong (M-1)^{Wkb} \cong \frac{\alpha_0 l_{cf} A}{\beta_0} (T_e^{Wk}(\Delta L^{Wk}) - T_0) \exp\left(-\frac{\beta_0}{A(T_e^{Wk}(\Delta L^{Wk}) - T_0)}\right) \quad . \qquad (3.15)$$

$\Delta L^{wk}$ is obtained from a quasi-2D analysis (please see APPENDIX B) in weak inversion to be,

$$\Delta L^{Wk} \cong l_{cf} \ln\left(\frac{L^2}{l_{cf}^2}\right) \quad . \qquad (3.16)$$

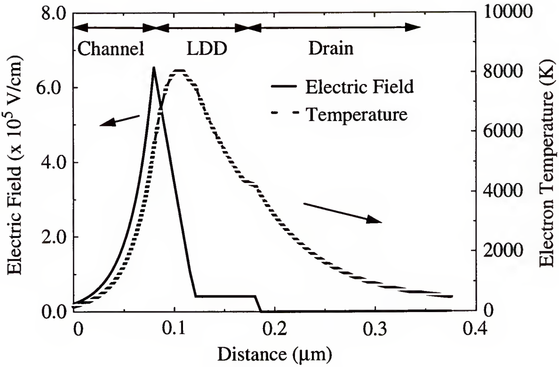


Fig. 3.2 SOISPICE-predicted electron temperature and electric field in an LDD (FD/SOI) MOSFET; $L = 0.2\ \mu m$.

The analyses for the LDD and the drain are analogous to those for strong inversion, except they are done at both surfaces.

### 3.2.2.2 PD/SOI

Impact ionization in weak-inversion in the PD/SOI MOSFET occurs in only the front surface, unlike that in the FD/SOI MOSFET. We first evaluate the field in the high-field region in weak inversion to be (Please see Appendix B.):

$$|E_f(y)| \cong 2\eta l_c \sinh\left(\frac{y}{l_c}\right) \quad , \tag{3.17}$$

where $l_c = t_b(C_b/(2C_{of}(1+\alpha)))^{1/2}$. The corresponding $T_e(y)$ and (M-1) can be obtained analogously to (3.14) and (3.15). The corresponding channel length modulation for the PD/SOI MOSFET in weak inversion is given by (Appendix B),

$$\Delta L^{Wk} \cong l_c \ln\left(\frac{L^2}{2l_c^2}\right) \quad . \tag{3.18}$$

### 3.2.3 Moderate-Inversion Analysis

In moderate inversion, it is not possible to analytically estimate the fields, as it is a transition region where suitable approximations and assumptions cannot be employed. However, based on the calculated multiplication factors in weak- and strong-inversion regions, we can interpolate to get a representative (M-1). The moderate-inversion (M-1) for both the FD/ and the PD/SOI MOSFET is interpolated as

$$(M-1)^{\text{Mod}} \cong \exp\left[\frac{\log\{(M-1)^{\text{Str}}\}(V_{TS}-V_{GfS}) + \log\{(M-1)^{\text{Wk}}\}(V_{GfS}-V_{TW})}{(V_{TS}-V_{TW})}\right] \quad . \qquad (3.19)$$

## 3.3 Model Implementation

The non-local characterization of $I_{Gi}$ in (3.1) is implemented in the SOISPICE [Fos95] FD/SOI and PD/SOI MOSFET model routines as post-processing. That is, the main model algorithms define E(y), as well as primary currents and charges, which in turn defines (M-1) as described in the preceding section. It is important to clarify the meaning of post-processing here. In a normal post-processing, e.g., in a device simulator [Med94], the main solution is independent of the post-processing. Here, however, they are coupled. For example, floating-body effects driven by the "post-processed" $I_{Gi}$, which is one of the currents in the network representation of the SOI MOSFET in Fig. 3.3, does affect the main solution. If impact ionization is requested, the main model routine first calculates the field for a given bias point, and then calls a subroutine which returns (M-1). The main model now returns $I_{Gi}$ (= (M-1)($I_{CH}$+$I_{BJT}$)) to SPICE, in addition to other currents. SPICE must now solve for the nodal equation at B' (body node) with $I_{Gi}$ included. Hence, after convergence at that bias point is obtained, the resulting $V_{B'S'}$ (and all other currents) will implicitly account for $I_{Gi}$, thereby properly incorporating $I_{Gi}$-driven effects.

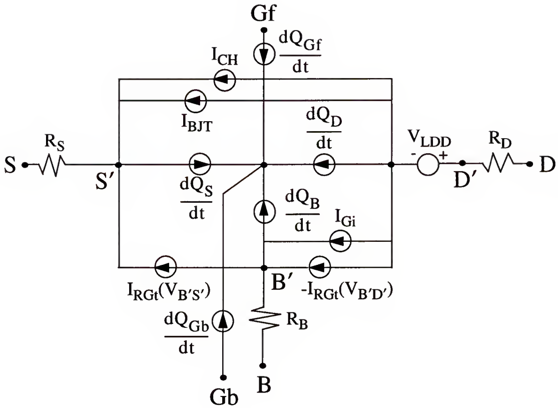


Fig. 3.3 Network representation of five-terminal charge-based models (FD and PD) in SOISPICE.

## 3.4 Verification and Discussion

Verification of the model cannot be done directly since the high body resistance in SOI MOSFETs precludes accurate measurement of $I_{Gi}$ as substrate current [Suh94]. One way to verify the model, albeit indirectly, is to predict the floating-body drain-source breakdown voltage, which is governed by impact ionization. The premature breakdown of the (n-channel) SOI MOSFET [Cho91] is caused by injection of holes generated by impact ionization that induce a forward bias on the body-source junction, thereby activating the parasitic BJT in the floating body as indicated in Fig. 3.4. The breakdown condition is reached when $\beta(M-1) \rightarrow 1$, where $\beta$ is the internal BJT gain given by $I_{BJT}/I_{Gi}$ for the floating-body device. Since local-field models overestimate (M-1), they predict this condition for breakdown at a drain-source bias smaller than the actual breakdown voltage. Contrarily, SOISPICE simulations track the breakdown voltage fairly well, even when the device structure is varied, and this tracking supports our non-local model for $I_{Gi}$.

Complementary support is provided by accurate predictions of saturation-region current kinks in floating-body PD/SOI devices. The kinks are also governed by impact ionization, being due to the (inverse) body effect defined at lower drain-source voltage by the body-source forward bias.

We discuss here this model verification based on measured breakdown and kink characteristics of a variety of deep-submicron n-channel FD and PD SOI MOSFETs. The SOISPICE model parameters were evaluated systematically without resorting to empirical optimization. Some measurement-based tuning was done (e.g., for flatband voltage), but most of the parameters, which are physical, were evaluated from knowledge of the device

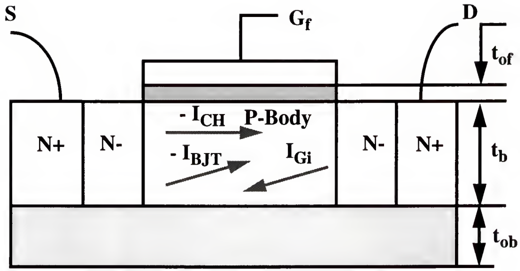


Fig. 3.4 Schematic which shows how impact ionization triggers the parasitic BJT in the floating body thereby causing premature drain-source breakdown in DC.

structure (e.g., body doping density). In accord with [Slo91], the values of impact-ionization coefficients in (3.6) for the simulations were assumed to be $\alpha_0 = 2.45 \times 10^6$ cm$^{-1}$ and $\beta_0 = 1.92 \times 10^6$ V/cm, and $\lambda_e = 650$ A (which agrees well with Monte Carlo simulations of carrier temperature under uniform field conditions [Slo91]) was used. In all the simulations, 1-D models for the parasitic BJT [Suh95] in the FD and PD devices were used. (Accounting for the 2-D nature of hole flow in the source and electron flow in the body could improve the accuracy of the breakdown predictions, especially for extremely short L.)

Fig. 3.5 shows the measured and SOISPICE-simulated current-voltage characteristics of an L = 0.3 μm FD/SOI MOSFET for different gate voltages. As shown, the simulated breakdown voltage is in good agreement with the measured data, especially at lower gate biases. The discrepancies between measured and simulated data at higher gate biases is caused by self-heating [Su94], which is not accounted for in our model. Self-heating not only reduces the output conductance, but also decreases the impact-ionization rate. Therefore, at higher gate biases the breakdown voltage predicted by our model is slightly smaller than the actual breakdown voltage.

The model also predicts breakdown well when the FD device structure is scaled.Fig. 3.6 shows how SOISPICE simulations track the breakdown voltage when the SOI film thickness is decreased. It must be pointed out however that the higher breakdown voltage seen for the thinner device is an artifact of a larger series resistance ($R_{S/D} = 195\ \Omega$ for $t_b = 53$ nm compared to $R_{S/D} = 50\ \Omega$ for $t_b = 90$ nm). To stress this fact, we have included in Fig. 3.6 the simulated data for the $t_b = 53$ nm device without the high series resistance. The direct dependence of the breakdown voltage on $t_b$ is thus seen to be weak, as was noted in

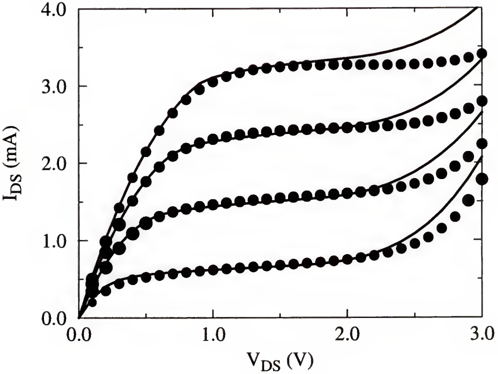


Fig. 3.5 Measured (points) and simulated (curves) $I_{DS}$-$V_{DS}$ characteristics of an L = 0.3 μm FD/SOI MOSFET for effective gate bias ($V_{GfS}$-$V_{Tf}$) varying from 0.5 V to 2.0 V; $t_b$ = 42 nm, $t_{of}$ = 9 nm.

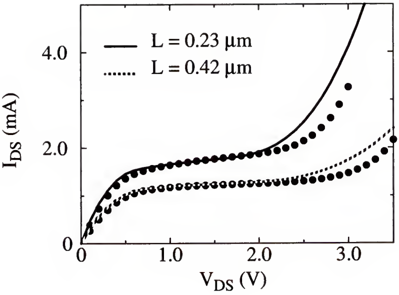


Fig. 3.6 Measured (points) and simulated (curves) $I_{DS}$-$V_{DS}$ characteristics of L ≅ 0.3 μm FD/SOI MOSFETs having different $t_b$; $(V_{GfS} - V_{Tf}) = 1.0$ V, $t_{of} = 11$ nm. Note that the higher breakdown voltage for the thinner device is an artifact of the large series resistance.

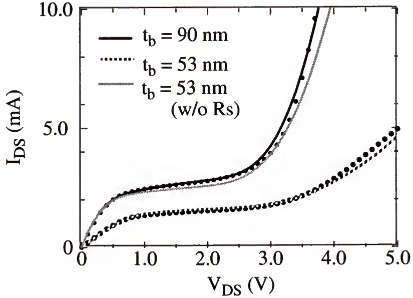


Fig. 3.7 Measured (points) and simulated (curves) $I_{DS}$-$V_{DS}$ characteristics of $t_b = 42$ nm FD/SOI MOSFETs having different L; $(V_{GfS} - V_{Tf}) = 1.0$ V, $t_{of} = 9$ nm.

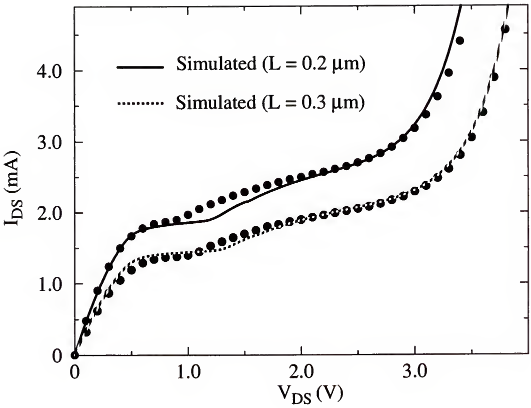


Fig. 3.8 Measured (points) and simulated (curves) $I_{DS}$-$V_{DS}$ characteristics of PD/SOI MOSFETs having different L; $V_{GfS} = 1.5$ V, $t_{of} = 5$ nm, $t_{b(eff)} = 50$ nm.

[Cho91]. The model also predicts the change in breakdown voltage as L is scaled, as shown in Fig. 3.7. The breakdown voltage is lower for the shorter device (L = 0.23 μm) mainly because of the larger $I_{BJT}$ and therefore a higher β [Cho91].

The model was also applied to predict breakdown and kinks in a PD/SOI technology as indicated in Fig. 3.8. The predicted breakdown voltages corresponding to scaled L are quite good, as are the kinks predicted at lower $V_{DS}$. The higher breakdown voltage for this technology relative to the FD one of Fig. 3.5 is mainly due to the thinner gate oxide, which means smaller threshold voltage, higher $V_{DS(sat)}$, and hence lower electric field [Cho91] and carrier temperature, and less impact ionization.

As indicated by the results in Figs. 3.5-3.9, the non-local model does seem to properly reflect the structural dependence of $I_{Gi}$. The model predictions in Fig. 3.9 show that (M-1) is relatively insensitive to the scaled FD/SOI film thickness, in general accord with numerical simulations accounting for non-local impact ionization [Ago94], but in contrast to the pessimistic prediction of the local-field model [Cho90]. The underlying reason for the insensitivity is that when the film thickness is scaled, the maximum field increases but so does the field gradient, causing the carrier temperature and consequently (M-1) to be relatively independent of film thickness. Consistent with this prediction, the breakdown voltage seems to be fairly independent of film thickness as exemplified in Fig. 3.7. These results suggest that ultra-thin (FD) films could be used for design optimization of deep-submicron SOI CMOS without exacerbating the effects of the parasitic BJT. Recent experimental results [Omu91] are consistent with this suggestion, whereas the local-field model predicts prohibitive BJT breakdown in ultra-thin-film SOI MOSFETs [Cho91].

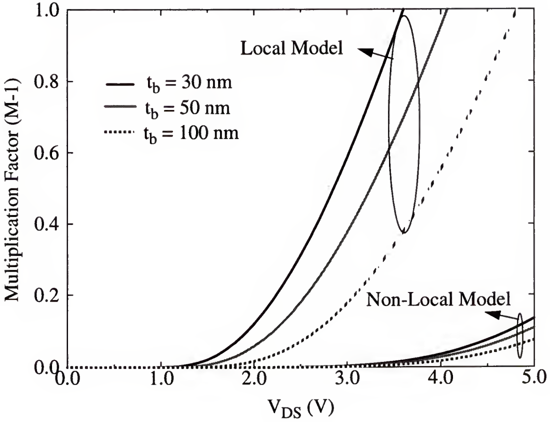


Fig. 3.9 Sensitivity to SOI film thickness of local-field and non-local models for impact ionization (M-1) in an FD MOSFET; L = 0.2 μm without LDD, $t_{of}$ = 7 nm.

## 3.5 Model Application to Device/Circuit Design Optimization

The predictive $I_{Gi}(T_e)$ model and SOISPICE are useful for design optimization as implied in the previous section. As channel lengths are scaled aggressively, the parasitic BJT-induced breakdown could be a possible "show-stopper" in the development of SOI technology. In this regard, the model can be used to check the efficacy of an LDD in scaled SOI CMOS devices and circuits. While use of an LDD increases the breakdown voltage, it decreases the device current drive and associated transconductance, and hence diminishes circuit speed. We present here examples of optimal CMOS device/circuit design that involve considerations of LDD tradeoffs between device breakdown and circuit speed.

We simulate actual FD and PD technologies with effective L scaled down to 0.2 μm. The FD device ($t_b = 50$ nm, $t_{of} = 5$ nm) corresponds roughly to Fig. 3.5; the PD device corresponds to Fig. 3.8. The expected supply voltage ($V_{DD}$) for a 0.2-μm technology is 2.5 V. The SOISPICE-predicted breakdown voltages, plotted in Fig. 3.10 versus the LDD doping, for both FD/SOI and PD/SOI are almost adequate for a $V_{DD} = 2.5$ V technology even without an LDD. To improve the safety margin (between breakdown voltage and supply voltage), a relatively heavily doped LDD could be used, costing not more than 10% loss in circuit speed as indicated by the SOISPICE-predicted gate propagation delays plotted in Fig. 3.11. (The slightly faster speeds predicted for the FD technology are due in part to the enhanced currents, lower threshold voltages, and smaller intrinsic gate capacitances.)

These examples seem to indicate that the need for an LDD is lessened in scaled technologies because of the non-local nature of impact ionization. Furthermore as L is scaled

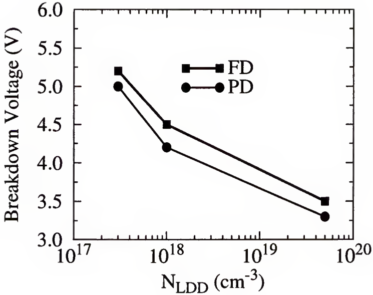


Fig. 3.10 SOISPICE-predicted breakdown voltage of (n-channel) FD/SOI and PD/SOI MOSFETs ($L = 0.2$ μm, $L_{LDD} = 0.1$ μm, $t_b = t_{b(eff)} = 50$ nm, $t_{of} = 5$ nm). The $N_{LDD} = 5 \times 10^{19}$ cm$^{-3}$ points represent no LDD.

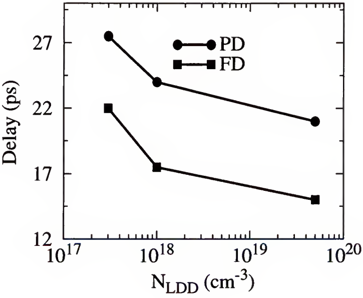


Fig. 3.11 Corresponding to Fig. 3.10, SOISPICE-predicted gate propagation delay of unloaded 3-stage CMOS inverter circuits ($V_{DD} = 2.5$ V) versus LDD doping density.

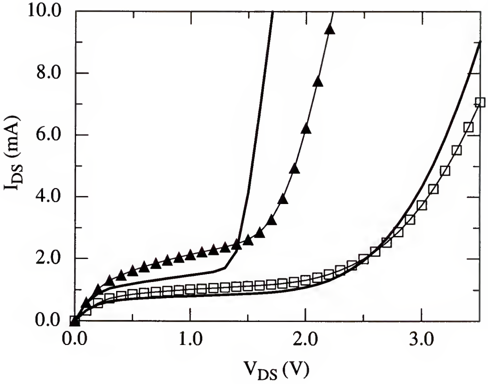


Fig. 3.12 SOISPICE-simulated breakdown as L is scaled from 0.2 μm (squares) to 0.1 μm (triangles); the solid curves represent simulations without overshoot; the improvement in breakdown for L = 0.1 μm is more than 0.5 V.

below 0.2 μm, another non-local phenomenon tends to further restrict impact ionization. Velocity overshoot, which was discussed in the previous chapter, implies a lower electric field and hence carrier temperature than inferred with local-field modeling of mobility for a specific drain bias $V_{DS}$. Preliminary analyses suggest that for L $\cong$ 0.1 μm the overshoot can produce a substantive reduction in impact ionization, especially at low $V_{DS}$, and hence ameliorate the parasitic BJT effects. SOISPICE simulations in Fig. 3.12 show a marginal improvement in breakdown voltage for a 0.2 μm device, whereas the improvement in breakdown voltage for a 0.1 μm device is improved by more than 0.5 V due to velocity overshoot. This suggests exploiting overshoot in scaled devices (L $\leq$ 0.1 μm) to improve breakdown as well as to enhance performance.

## 3.6 Conclusions

It has been shown in this chapter that non-local modeling of impact ionization is essential for predicting breakdown and kinks in scaled floating-body SOI MOSFETs. Contrary to local-field models, the non-local model developed here predicts that the multiplication factor due to impact ionization is relatively insensitive to scaled SOI film thickness. The non-local model, implemented in SOISPICE and supported by measurements of breakdown and kinks in a variety of FD/SOI and PD/SOI device structures, can hence be used to comprehensively study $I_{Gi}$-driven floating-body effects at the device and circuit levels, as well as to help characterize the parasitic BJT which can be important even at voltages well below breakdown [Pel95]. In this regard, SOISPICE-aided design optimization of deep-submicron SOI CMOS technologies, for example, for effecting a good tradeoff between device breakdown and circuit speed, were illustrated. The need for an LDD in scaled SOI technologies was assessed; its efficacy seems to be unwarranted in deep-submicron technologies because of the non-local nature of impact ionization, and, for L < 0.2 μm, possibly velocity overshoot. Designing FD or PD to exploit these non-local effects thus seems to be worthy of consideration. It is important to note that (sub-threshold and strong-inversion region) kinks driven by impact ionization will still occur at voltages well below breakdown. The subthreshold kink can possiby increase the off-state current in low-voltage applications, depending on the threshold voltage. Until recently, only the PD/SOI MOSFET has been known to exhibit this kink. In the next chapter we show that a subthreshold kink driven by impact ionization can occur in FD/SOI MOSFETs, and we use a physical model to explain this effect. We also consider possible design to suppress this kink.

# CHAPTER 4
# FLOATING-BODY KINKS AND DYNAMIC EFFECTS IN FULLY DEPLETED SOI MOSFETs

## 4.1 Introduction

As SOI CMOS technology matures, floating-body effects in the SOI MOSFET remain a critical issue [Yos94]. The premature breakdown and latch caused by the parasitic bipolar transistor [Cho91] are well known examples of these effects that plague both fully depleted (FD) and partially depleted (PD) devices, but the current kinks and the dynamic instabilities in circuits caused by the sensitivity of threshold voltage to the floating body-source bias [Suh94b] are generally associated with the PD/SOI technology [Kad94]. Recently however Pelloie and Sun [Pel94] showed that a kink effect could occur in an FD device if the SOI film is not everywhere "deeply depleted".

In this chapter, extending [Pel94], measured characteristics of scaled FD/SOI MOSFETs showing subthreshold kinks are presented. Aided by analytical device modeling and simulation, the underlying physical mechanism is described, explaining how it differs from the PD/SOI kink effect. This gives insight that qualifies the meaning of FD/SOI and implies new design issues regarding off-state current for low-voltage FD/SOI CMOS technology.

## 4.2 Device Measurements

The measured enhancement-mode n-channel SOI (SIMOX) MOSFETs designed at LETI have gate lengths scaled to 0.2 μm (effective L scaled to 0.15 μm). The floating-body devices are in ultra-thin SOI films of 30 and 50 nm with very high body doping (of about $1 \times 10^{18}$ cm$^{-3}$), achieved by a single boron implantation. They have front and back oxide thicknesses of 4.5 and 380 nm, respectively, and include LDDs (doped to about $2 \times 10^{18}$ cm$^{-3}$).

Whereas the thicker-film devices are PD, the 30-nm devices are classically FD; they reflect strong coupling between the front and back gates [Lim83] as exemplified by the linear-region data plotted in Fig. 4.1 for an L = 0.25 μm device. The front-channel threshold voltage, nominally about 0.4 V, increases with decreasing back-gate (substrate) bias for $V_{GbS}$ as low as -20 V. Furthermore the low-$V_{DS}$ subthreshold swing (S) evident in the data plotted in Fig. 4.2 is close to the lower limit of 60 mV, which is also characteristic of the FD mode [Col91]. In strong inversion, the thinner-film devices show no current kinks, which is indicative of FD too [Col91].

Figure 4.3 shows the subthreshold $I_{DS}$-$V_{GfS}$ characteristics measured at low and high $V_{DS}$. Note that the high $V_{DS}$ (= 2.5 V) is well below the latch and breakdown voltages (of about 3.5 V) of the L = 0.25 μm device. The high-$V_{DS}$ characteristics show kinks reflecting large increases in current over a wide range of $V_{GfS}$ similar to the kink in PD/SOI MOSFETs [Fos87]. Evidently, impact ionization, which underlies the kink, injects holes into the body that alters its charge condition [Che94], perhaps converting it from FD to PD. However this theory is not consistent with the $V_{GbS}$ dependence of the characteristics

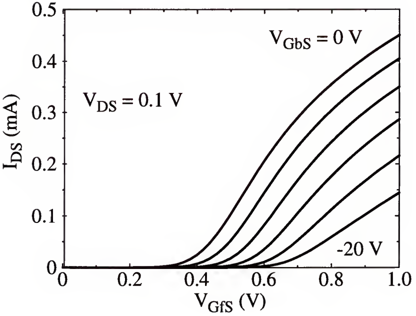


Fig. 4.1 Measured linear-region current-voltage characteristics of a scaled L = 0.25 µm FD/SOI MOSFET (with LDD) at low $V_{DS}$ (= 0.1 V) for different values of back gate (substrate)-source bias ($V_{GbS}$ = 0 to -20 V). Note that the threshold voltage increases with decreasing $V_{GbS}$.

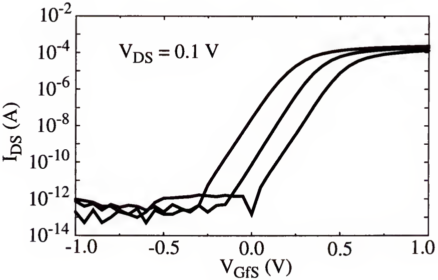


Fig. 4.2 Measured subthreshold-region current-voltage characteristics at low $V_{DS}$ (= 0.1 V) corresponding to device of Fig. 4.1 for different $V_{GbS}$ (+10 V, 0, -10 V). The subthreshold swing is approximately ideal (≈ 60 mV/dec) for all $V_{GbS}$.

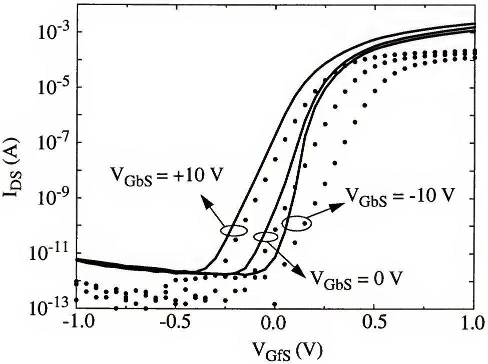


Fig. 4.3 Measured subthreshold-region current-voltage characteristics at (high) $V_{DS}$ = 2.5 V (solid curves) corresponding to device of Fig. 4.1 for different $V_{GbS}$ (+10 V, 0, -10 V). Note that the kink is absent for $V_{GbS}$ = +10 V, but grows as $V_{GbS}$ decreases. The low $V_{DS}$ curves (points) are included for reference.

seen in Figs. 4.1 and 4.2. The dependence is strong, signifying the prevalent FD mode, even though the PD-like subthreshold kink materializes and grows as $V_{GbS}$ is decreased from +10 to -10 V.

## 4.3 Analysis

The basic mechanism underlying the kink effect in PD/SOI MOSFETs [Col91, Fos87] is well known. Majority holes, generated by impact ionization, are injected into the neutral portion of the body (Fig. 4.5) and induce a forward bias $V_{BS}$ on the body-source junction. The threshold voltage is thus lowered via the (inverse) body effect, and the channel current increases as illustrated in Fig. 4.4(a) and Fig. 4.4(b).

The underlying mechanism in the FD/SOI MOSFET (schematic shown in Fig. 4.6) is different since there is no neutral body region. To describe it and the kinks in Fig. 4.3, we must consider the carrier distributions in the "depleted" body, and qualify the meaning of FD. In accord with the classical gate-coupling theory [Lim83], FD means any degree of depletion for which the carrier densities (p and n) are much lower than the body doping density $N_A$; but it does not mean $p = n = 0$. For a low-$V_{DS}$ weak-inversion condition then, Poisson's equation defines the electrostatic potential $\psi$, illustrated in Fig. 4.7 across the SOI film body, and Gauss's law relates the front and back surface potentials $\psi_{sf}$ and $\psi_{sb}$ to the gate biases $V_{GfS}$ and $V_{GbS}$ [Lim83]; and $p \equiv p_o = n_i^2/n_o = N_A\exp(-q\psi/kT) \ll N_A$.

For high $V_{DS}$, impact ionization injects more holes into the FD body. The excess holes ($\Delta p$) accumulate near the source and induce $V_{BS} > 0$, which enables electron ($\Delta n$) injection from the source. Results of steady-state numerical simulations in Fig. 4.8 show that

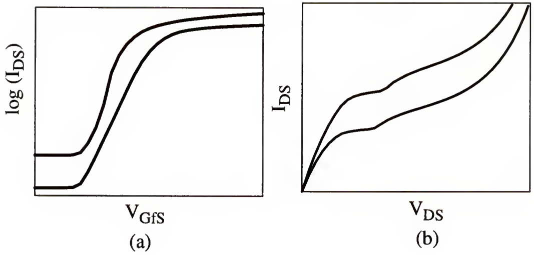


Fig. 4.4 Typically seen kinks in subthreshold (a) and strong-inversion (b) regions in PD/SOI MOSFETs.

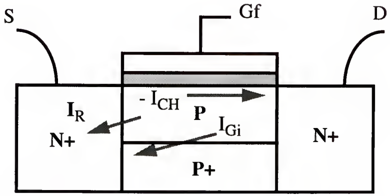


Fig. 4.5 Schematic of PD/SOI MOSFET. The neutral (P+ layer here) body is responsible for impact-ionization driven kinks in Fig. 4.4 via the (inverse) body effect.

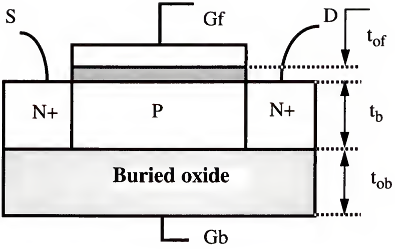


Fig. 4.6 Schematic of an FD/SOI MOSFET. The P-body for an FD/SOI is always depleted, even though the "degree" of depletion can vary depending on the structure as well as the back-gate bias.

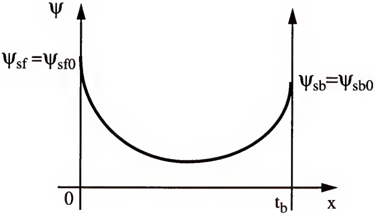


Fig. 4.7 Potential distribution (at low $V_{DS}$) in an FD/SOI MOSFET in the vertical direction (solved from Poisson's equation with boundary conditions from Gauss's law). $\psi_{sf0}$ and $\psi_{sb0}$ are the low-$V_{DS}$ potentials at the front and back surface respectively.

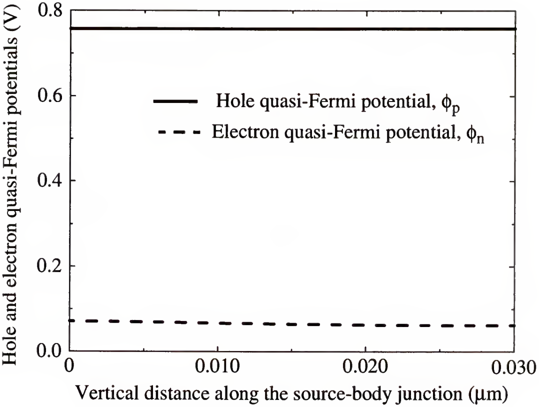


Fig. 4.8 MEDICI-simulated hole and electron quasi-Fermi potentials along the junction (in the vertical direction) for a FD/SOI MOSFET. The difference between these two potentials is nearly a constant indicating the presence of a uniform source-body junction bias $V_{BS}$ ($\equiv \phi_p$-$\phi_n$). This further implies from (4.1) that the pn product is constant. The structure of the simulated device corresponds to the FD/SOI MOSFET in Fig. 4.1.

$V_{BS}$, which is defined by the equivalence of the carrier generation and recombination currents in the device [Cho91], is nearly uniform along the source junction in accord with a vertical (x-direction) detailed balance; the simulations further confirm that dielectric relaxation forces $\Delta n \cong \Delta p$. Thus along the body-source junction [Sze81],

$$pn \cong (p_o + \Delta p)(n_o + \Delta p) \cong n_i^2 \exp\left(\frac{qV_{BS}}{kT}\right) \quad . \tag{4.1}$$

The injected electrons constitute the parasitic bipolar transistor current, which is distinguished from the channel current by its $\exp(V_{BS}/kT)$ dependence. At sufficiently high $V_{DS}$ this strong dependence supports regeneration of the bipolar current which underlies the subthreshold latch (and breakdown) [Cho91]. The kinks in Fig. 4.3 occur at lower $V_{DS}$ and are stable, and they are sensitive to $V_{GbS}$, which does not significantly affect the bipolar current. Therefore the bipolar current must not be predominant, and the kinks are mainly increases in channel current that result from a perturbation of $\psi$ defined by $V_{BS}$.

The perturbation of $\psi$ is two-dimensional. Our numerical simulations predict it, but the results are difficult to interpret physically. To get an analytical understanding of the perturbation effect, consider the energy-band diagrams in Figs. 4.9 and 4.10 drawn across the body-source junction at the back surface ($x = t_b$). The carrier quasi-Fermi levels are separated by $V_{BS}$ [Sze91], thus defining a reduction of the energy barrier and an increase $\Delta\psi_{sb}$ of the back surface potential as indicated. The gate-coupling theory [Lim83] then implies the corresponding increase in front-surface potential, $\Delta\psi_{sf} \cong [C_b/(C_b+C_{of})] \Delta\psi_{sb}$ where $C_{of}$ is the front-gate oxide capacitance and $C_b = \varepsilon_s/t_b$. (Because of the two-dimensionality of the effect, this approximation as well as Figs. 4.9 and 4.10 are not exact,but are representative.) The channel current ($I_{DS} \propto \exp(q\psi_{sf}/kT)$) increases as

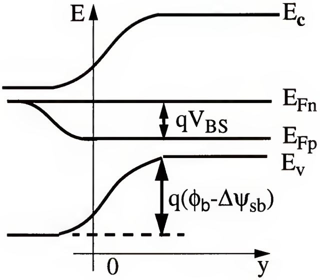


Fig. 4.9 Energy-band diagram across (in the horizontal y-direction) the source-body junction at the back surface ($x = t_b$) of the SOI film body for a "strongly FD" mode of operation. Also shown are the quasi-Fermi levels. The low-$V_{DS}$ barrier $\phi_b$ is unchanged as $\Delta\psi_{sb} \approx 0$ since the device is "strongly" depleted. For this case, the conduction and valence bands do not respond for a given separation of quasi-Fermi levels. The energy bands are hence "rigid".

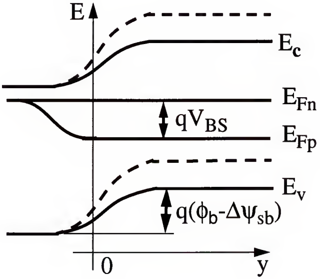


Fig. 4.10 Energy-band diagram across the body-source junction when the SOI film body is "mildly" depleted. For this case, the conduction and valence bands follow the quasi-Fermi level separation, i.e., $\Delta\psi_{sb} \approx V_{BS}$. The dashed lines show the conduction and valence bands under equilibrium (or low-$V_{DS}$) conditions.

defined by $\Delta\psi_{sf}$, and a kink materializes, the magnitude of which is governed by $V_{BS}$ and the dependence of $\Delta\psi_{sb}$ on it.

We can get more physical insight from this quasi-two-dimensional analysis by checking two extreme FD/SOI MOSFET modes defined by the low-$V_{DS}$ hole density

$$p_o(t_b) = N_A \exp\left(-\frac{q\psi_{sb}}{kT}\right) \quad . \tag{4.2}$$

First, if $p_o(t_b)$ is extremely low (viz., for a *strongly* FD body), $\psi_{sb}$ is large and $n_o(t_b)$ is relatively high. In this case, (4.1) gives $\Delta p \cong \Delta n \ll n_o(t_b)$; hence $n(t_b)$ is virtually constant, and the energy bands in Fig. 4.9 are rigid, independent of $V_{BS}$. So $\Delta\psi_{sb}$ is negligible, and the kink is suppressed. This mode underlies the $V_{GbS} = +10$ V characteristic in Fig. 4.3, which shows no kink. Second, if $p_o(t_b)$ is relatively high (viz., for a *mildly* FD body), $\psi_{sb}$ is first small. Then $\Delta p \ll p_o(t_b)$; so $p(t_b)$ is virtually constant, and the energy bands in Fig. 4.10 track the hole quasi-Fermi level. Hence $\Delta\psi_{sb} \cong V_{BS}$, and the kink is most significant. This mode underlies the $V_{GbS} = -10$ V characteristic in Fig. 4.3, which shows a pronounced kink. Note that it resembles the PD mode [Col91], for which the limit of $p_o(t_b) \rightarrow N_A$ without $V_{GbS}$ dependence applies.

## 4.4 Modeling

### 4.4.1 Introduction

Previous modeling of the FD/SOI [Yeh95] MOSFET in SOISPICE assumes that the potentials (at the front and back surface) are independent of $V_{BS}$, which in turn makes the threshold voltage independent of $V_{BS}$. While this assumption is valid for the "strongly FD" mode of operation, it is incorrect for the "mildly FD" mode, which can result in the subthreshold kink. Hence, to assess design trade-offs due to the above mentioned kink, a physical model that accounts for the variation of surface potential due to $V_{BS}$ is necessary. Here we outline the development of the needed model.

### 4.4.2 Model Development

The model development is based on characterization of the low-$V_{DS}$ hole density $p_o(t_b)$ described by (4.2), which defines the degree of depletion, and the pn product at the source-body junction described by (4.1). The assumptions made here are:

(i) $p_o(t_b)$ can be adequately characterized by solution of 1-D Poisson's equation (with boundary conditions implied by Gauss's law);

(ii) pn product along the junction is a constant;

(iii) $\Delta p(x) \approx \Delta n(x)$ along the body-source junction.

The first assumption is true in the mildly FD mode of operation, where fringing due to 2-D fields [Yeh93] will tend to be small, while the second assumption is forced by vertical detailed balance as verified by 2-D MEDICI simulations reflected in Fig. 4.8. Further, dielectric relaxation in the body-source junction will dictate a quasi-neutral-like condition where the excess carrier densities tend to be nearly equal.

With these assumptions, then $\Delta p(x = t_b)$ ($\approx \Delta n(x = t_b)$) can be evaluated as

$$\Delta p(t_b) \cong \Delta n(t_b) = \frac{\left(-(p_o(t_b)+n_o(t_b)) + \sqrt{(p_o(t_b)+n_o(t_b))^2 + 4n_i^2\exp\left(\frac{V_{BS}}{V_T}\right)}\right)}{2} \tag{4.3}$$

where $n_o(t_b) = n_i^2/p_o(t_b)$.

The resulting hole density $p(t_b)$, at any given $V_{BS}$, is expressed as

$$p(t_b) = \frac{\left(\{p_o(t_b)-n_o(t_b)\} + \sqrt{\{p_o(t_b)+n_o(t_b)\}^2 + 4n_i^2\exp\left(\frac{V_{BS}}{V_T}\right)}\right)}{2} \quad . \tag{4.4}$$

Further, from pn junction theory and Boltzmann's approximation for carrier densities, $p(t_b)$ can be expressed as

$$p(t_b) = p_o(t_b)\exp\left(\frac{-q(\Delta\Psi_{sb} - V_{BS})}{V_T}\right). \tag{4.5}$$

Equating (4.4) and (4.5) yields a relationship between $\Delta\psi_{sb}$ and $V_{BS}$. Now, to complete the model formalism, the coupling between $\Delta\psi_{sf}$ and $\Delta\psi_{sb}$ must be known. This can be obtained from an analysis following [Lim83] to be

$$\Delta\psi_{sf} \approx \Delta\Psi_{sb}\left(\frac{C_b}{C_b + C_{of}}\right) \quad . \tag{4.6}$$

The above expression accounts physically for the fact that any perturbation of $\Delta\psi_{sb}$ due to a change in $V_{BS}$ affects $\Delta\psi_{sf}$. Now any change in $\Delta\psi_{sf}$ will affect channel current (due to threshold lowering), since the channel current, as indicated earlier, is proportional to $\exp(q\Delta\psi_{sf}/kT)$.

## 4.5 Application to Design

The occurrence of the subthreshold kink in FD/SOI MOSFETs portends dynamic floating-body charging effects as in PD/SOI devices and circuits [Suh94b]. However numerical 2-D simulations (Fig. 4.11) with TMA- MEDICI, tuned to the LETI device of Figs. 4.2 and 4.3 suggest that the $V_{Tf}(t)$ transients resulting from $V_{GfS}(t)$-induced body charging are negligible. These device simulations, and transient circuit simulations with SOISPICE, reveal that as long as the body is FD, irrespective of the degree of depletion and the prevalence of a kink, the body charge fluctuation is minimal, and FD/SOI CMOS circuits tend to be free of the associated dynamic instabilities.

The kink can result in abnormally high off-state current ($I_{off}$) in low-voltage applications though. For example, if the LETI device is scaled, the kink would tend to shift to the $V_{GfS} = 0$ V axis. However if such a lowering of $V_{Tf}$ requires reducing $N_A$, a strongly FD condition could obtain and suppress the kink; but source/drain charge sharing and field fringing in the BOX, which increase S [Yeh93], could be enabled too. Such scaling thus results in an unavoidable increase of $I_{off}$ as shown by the SOISPICE predictions in Fig. 4.12. Optimal low-voltage FD/SOI design will have to balance the effects of the kink and the charge sharing to minimize $I_{off}$. Our modeling of the kink, supported by MEDICI, gives needed design insight. As indicated in Fig. 4.12, thinning $t_b$ as well as reducing $N_A$ tend to yield a strongly FD condition that suppresses the kink. However, thinning the BOX is not effective, and even though thinning the gate oxide, which diminishes the gate coupling, is, the required device scaling seems quite aggressive and in need of innovation in the FD/SOI technology.

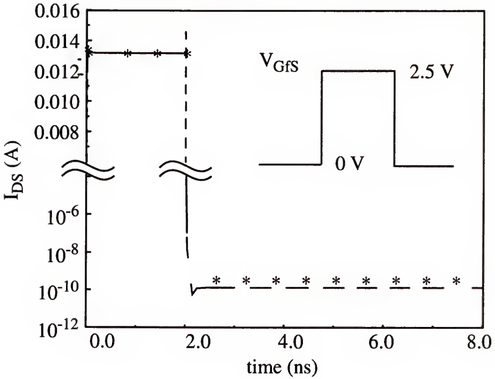


Fig. 4.11 MEDICI-simulated transient drain current resulting from turn-on and turn-off $V_{GfS}$ pulses on the device of Fig. 4.3; $V_{DS}$ = 2.5 V. The predicted steady-state on- and off-currents (points) are superimposed for comparison.

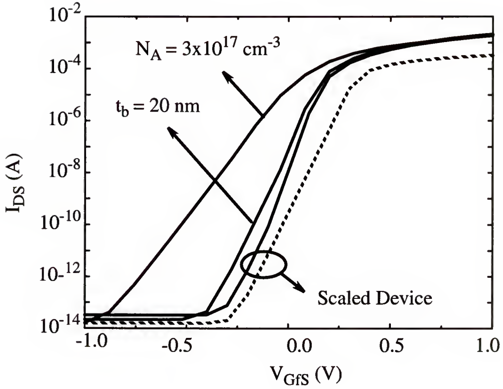


Fig. 4.12 SOISPICE-simulated subthreshold characteristics of a scaled version (W/L = 40μm/0.15μm, $N_A = 10^{18}$ cm$^{-3}$, $t_b = 30$ nm, no LDD) of the device of Figs. 4.1-4.3 at low $V_{DS}$ (= 0.1 V: dashed curve) and high $V_{DS}$ (= 1.5 V: solid curves); and predicted parametric dependences. Note how the kink tends to disappear when either $N_A$ or $t_b$ is scaled.

## 4.6 Conclusions

Subthreshold kinks can occur in *mildly* FD/SOI MOSFETs at $V_{DS}$ well below the breakdown and latch voltages. They are driven by impact ionization which induces a $V_{BS}$ that implicitly defines an increase of $\psi_{sf}$ via a two-dimensional perturbation of $\psi$ in the SOI film body. The underlying effect *does not involve the parasitic bipolar transistor.* The severity of the effect depends on the degree of depletion, i.e., on $p_o(t_b)$ in (4.2); the kink is suppressed when the body is *strongly* FD. Lowering $N_A$, thinning $t_b$, or (actually or effectively) increasing $V_{GbS}$ will tend to deplete the body and suppress the kink. Enhancing carrier recombination in the device will do so as well by limiting $V_{BS}$. Scaling L will tend to exacerbate the kink, as our measurements confirm, as the impact-ionization current increases with channel current.

The subthreshold kink can cause abnormally high $I_{off}$ in the FD/SOI MOSFET in low-voltage CMOS applications, depending on the threshold voltage. The results here suggest that $I_{off}$ can be high in FD/SOI MOSFETs because of a kink and/or charge sharing, and hence control of it may require harder design tradeoffs than previously thought [Yeh93].

In low-voltage applications, it has been recently shown [Pel95] that another floating-body effect, independent of impact ionization can be significant. The parasitic bipolar transistor can be activated at voltages well below breakdown due to dynamic body charging. To understand as well as characterize this effect for reliable circuit simulation, a physical bipolar model is necessary. This is the focus of the following chapter.

# CHAPTER 5
# PARASITIC BIPOLAR JUNCTION TRANSISTOR IN SOI MOSFETs: BIMOS MODELING, VERIFICATION, AND APPLICATION TO RELIABLE CIRCUIT DESIGN

## 5.1 Introduction

Recent work has clearly revealed that transient current in the parasitic bipolar junction transistor (BJT) of the floating-body SOI MOSFET can be significant [Pel95] and degrading [Suh96] even in SOI circuits operating at voltages well below the BJT-defined drain-source breakdown. The BJT is also critically important with regard to soft errors in low-voltage SOI memory circuits [Tos95]. In SOI DRAMs, the activation of the parasitic BJT can result in loss of stored charge in the cell capacitor, whereas in the SRAM, the stored data can be inverted. In these cases, the BJT current is driven by dynamic charging of the body and concomitant forward biasing of the source (or drain) junction, supported by capacitive, or charge coupling between the BJT and the MOSFET.

A reliable circuit model for the floating-body SOI MOSFET must therefore account for the coupled BJT. The parasitic BJT model in the current version (Ver. 4.3) of SOISPICE is inadequate, as it does not correctly account for the structural dependences (e.g., on channel length L), as well as the possible gate dependence, of the transient BJT current. In this chapter, a new, quasi-2D parasitic BJT model physically coupled to the SOISPICE [Fos95] MOSFET models and defined in terms of their parameters, is presented. Further, physical insight derived from this *BiMOS modeling* is used to identify a new means of controlling the transient BJT current in SOI MOSFETs and circuits which could be exploited in design.

## 5.2 The Transient Bipolar Effect

It is well known that the parasitic BJT is responsible for premature drain-source DC breakdown in scaled SOI MOSFETs [Cho91]. As mentioned in Chapter 3, the breakdown in DC is driven by impact ionization, which activates the parasitic BJT. It was hence thought that when the supply voltage is lowered, the parasitic BJT effect would be mitigated. However, recent work [Pel95] has shown that during low-voltage transients the BJT in pass transistors can indeed be activated.

The mechanism which activates the transient bipolar effect is dynamic body charging induced by charge (or capacitive) coupling between the parasitic BJT and the MOSFET, as schematically illustrated in Fig. 5.1. For example, the BJT can be driven by body charging due to a transition in the source. To understand the transient charge dynamics that drives the BJT, consider an n-channel PD/SOI MOSFET in a pass-gate configuration as shown in Fig. 5.2. Initially, the front-gate (Gf) is held at 0 V, and the source and drain are both held at $V_{DD}$ (well below the breakdown voltage). Assuming that the device has been sitting idle for a long time (>> $\tau_g$, the generation lifetime), the initial $V_{BS}$ (= $V_{BD}$) is zero since the *net* recombination and generation currents in the device are zero ($V_{DS}$ = 0) for this bias condition. This situation can exist, for example, in a DRAM pass transistor. Now, if a voltage transition occurs on the source (from $V_{DD}$ to 0), a large $V_{BS}$ is induced, which injects minority carriers into the body. These carriers are subsequently transported to the drain

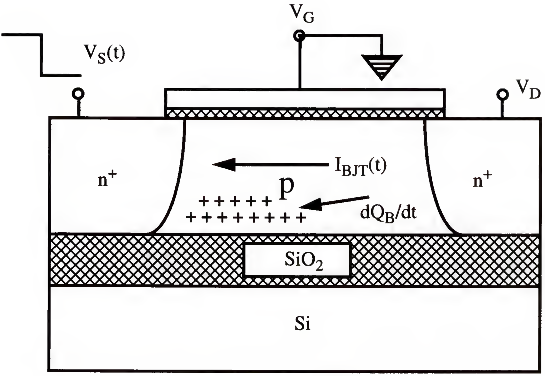


Fig. 5.1 Schematic diagram which illustrates how transient body-charging can trigger the parasitic bipolar in SOI MOSFETs.

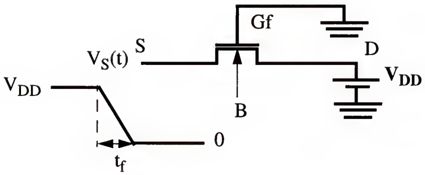


Fig. 5.2 Schematic of a PD/SOI pass-transistor circuit with a floating body; the fall time of the source-voltage pulse is $t_f$.

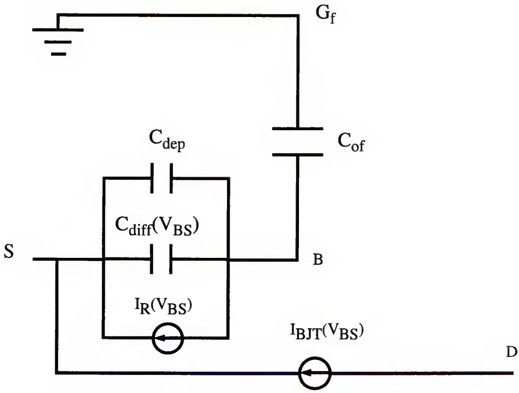


Fig. 5.3 Approximate equivalent circuit of the pass transistor in Fig. 5.2 to explain the transient BJT effect. Note that the initial $V_{BS} = 0$, if the device is idle for a long time. Otherwise for this bias condition, initial $V_{BS} < 0$, and is dependent on the period of $V_S(t)$.

which constitutes a transient bipolar current. The reason for the large increase in $V_{BS}$ can be qualitatively understood from Fig. 5.3, where the (approximate) equivalent circuit of the floating-body SOI MOSFET (for this switching condition) is shown. Initially, when the source-voltage pulse $V_S(t)$ falls, the front-oxide capacitance $C_{of}$ is much larger than the sum of the depletion and diffusion capacitances ($C_{dep}$+$C_{diff}(V_{BS})$) of the body-source junction. Since the voltage across a larger capacitance cannot change as rapidly as that across a smaller capacitance, $V_{GfB}$ (across $C_{of}$) varies slowly, while $V_{BS}$ (across $C_{dep}$ and $C_{diff}$) changes quickly. In other words, the voltage at node B, $V_B$, changes slowly. As $V_S(t)$ keeps falling, the build up in $V_{BS}$ continues until recombination and/or increasing diffusion capacitance set in to restrict any further increase in $V_{BS}$. Note that, usually, the peak of $V_{BS}$ (and $I_{BJT}(t)$) will correspond to the point in time after the fall of $V_S(t)$, as that is where the input swing ($V_{GfS}$) would be a maximum. After the fall of the pulse, the excess carriers will be removed at a rate governed by the recombination current and the diffusion capacitance. It is important to note that the magnitude of $I_{BJT}(t)$ is dependent on the period of $V_S(t)$, i.e., the effect is hysteretic [Pel95, Suh94b]. Basically, if $V_S(t)$ is switched rapidly ($T << \tau_g$) the body will not have adequate time to replenish carriers via thermal generation; consequently, the initial $V_{BS}$ *before* $V_S(t)$ drops again will be negative (as opposed to zero for a steady-state condition). Hence, the peak $V_{BS}$ (and $I_{BJT}(t)$) *after* $V_S(t)$ falls again will be smaller than its value corresponding to a drop after the steady-state condition obtains ($T >> \tau_g$).

The transient bipolar effect described here demands a physical bipolar model for reliable SOI circuit design. We discuss the development of a comprehensive model for this effect in the following section.

## 5.3 BiMOS Modeling

### 5.3.1 Introduction

In order to better understand, and possibly control the transient bipolar effect in scaled PD/SOI technologies, a physical model that characterizes (minority) carrier injection and transport for the parasitic BJT is needed. Further, the model must also properly account for the accompanying charges (e.g., stored diffusing charge), which as described in the previous section, are very crucial in controlling the dynamics of the transient BJT. Since the parasitic bipolar model is coupled to the SOI MOSFET, it will be referred to as a *BiMOS* model. As will be described later, the BiMOS modeling enables reliable parameter evaluation as well.

Fig. 5.4 shows the base structure of a PD/SOI MOSFET (used for model derivation), whose network representation was shown in Fig. 3.3. The basic physical, charge-based model for the MOSFET, including retrograde channel doping, has already been developed and extensively verified [Suh95]. The components in Fig. 3.3 for which new modeling will be applied are the parasitic bipolar transport current $I_{BJT}$, the recombination current $I_R$, and the bipolar components of the terminal source, drain, and body charges, $Q_S$, $Q_D$, and $Q_B$. Extension of the parasitic BJT model to the FD/SOI MOSFET is also outlined.

### 5.3.2 A Quasi-2D Model for the Parasitic Bipolar Transport Current

Before we detail the modeling for $I_{BJT}$, it is important to understand whether the transport of $I_{BJT}$ is one- or two-dimensional. The answer depends upon the inversion condition of the channel as discussed below.

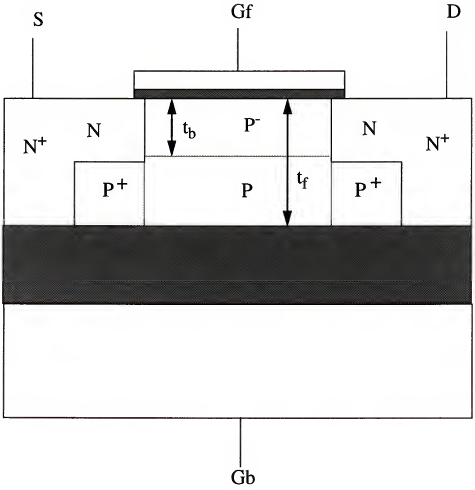


Fig. 5.4 Base structure assumed for the (n-channel) PD/SOI MOSFET for model derivation. The (vertical) body doping is modeled to be a hi-lo junction. All doping densities in the figure are assumed uniform in each region [Suh95].

### 5.3.2.1 BJT Transport Modeling: 1-D or 2-D?

The parasitic bipolar current in the SOI MOSFET can flow in one or two dimensions depending on the inversion condition in the channel. For example, in strong inversion, near breakdown (in DC) the current flows predominantly in the vertical direction. The reason for the vertical flow for this case is because the channel acts as an *extended* drain that collects injected minority carriers. Once the minority carriers are collected by the reverse-biased channel, they are subsequently transported to the drain. This is exemplified by MEDICI simulations near breakdown (in DC) illustrated in Fig. 5.5, where current flowlines are plotted. As can be clearly seen the flow is predominantly 2-D, due to strong inversion condition in the channel. It is tempting, therefore, to argue that a 2D-flow model for $I_{BJT}$ is necessary, i.e.,

$$\overline{J_{BJT}}(x, y) = J_{xBJT}(x, y)\bar{x} + J_{yBJT}(x, y)\bar{y} \quad , \tag{5.1}$$

and

$$I_{BJT} = \iint J_{xBJT}(x, y)dxdy + \iint J_{yBJT}(x, y)dxdy \quad , \tag{5.2}$$

where $J_{xBJT}$ and $J_{yBJT}$ are the x (vertical) and y (horizontal) components of the bipolar current densities.

However, for switching conditions where the *transient* bipolar current is of interest, the transport is not 2-D; the reason being that the transient bipolar effect is typically important when the device is *not* in strong inversion. Transient MEDICI simulations of a pass transistor illustrated in Fig. 5.6 show that for typical switching conditions the flow is 1-D (and nearly uniform for this example). When the channel is not strongly inverted, the

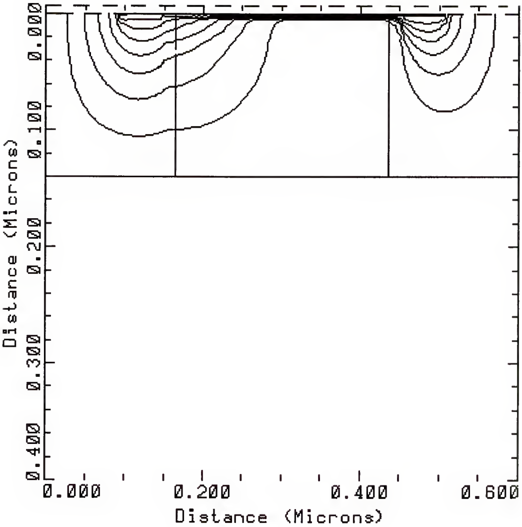


Fig. 5.5 MEDICI-simulated current flowlines in DC for a PD/SOI MOSFET near breakdown. The device was biased in strong inversion. Note 2-D flow due to the channel acting as a sink for injected minority carriers.

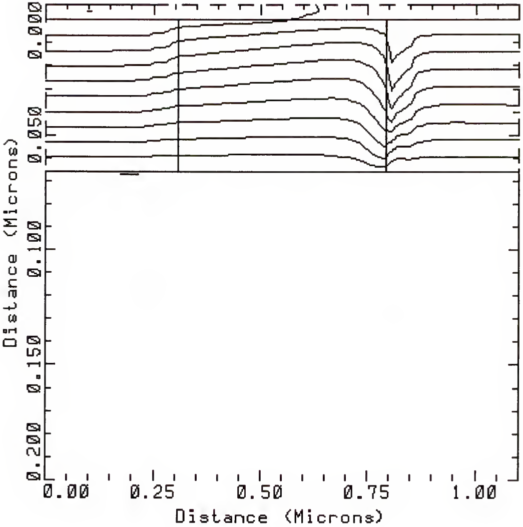


Fig. 5.6 MEDICI-simulated current flowlines of a PD/SOI MOSFET during a transient. The source was pulsed from 1.5 V to 0 V. The drain was held at 1.5 V, while the front-gate was held at 0 V. The flow is nearly uniform and 1-D. The flowlines here are plotted the instant $V_S(t)$ reaches 0 V.

injected carriers diffuse to the reverse-biased drain, and not towards the channel, even though there can be a net vertical field. The important point is that unless $pn \ll n_i^2$ in the channel close to the point of injection (i.e., the channel is reverse biased), the carriers diffuse towards the drain, or flow laterally, "ignoring" the effect of the possible presence of a vertical field.

There is, however, an important effect of the vertical field. A vertical field, which can be present when the gate-body bias ($V_{GfB}$) is increased beyond flatband, i.e., $V_{GfB}>V_{FB}$, serves to decrease the majority-hole density (or the Gummel number) in an n-channel MOSFET. This not only increases the BJT current density, but also results in current "crowding" near the surface as illustrated in Fig. 5.7. This gate dependence of the bipolar current can be important in devices which have a low flatband or threshold voltage. It is important not to confuse this gate dependence of bipolar current with the onset of channel formation, and current, even though there is a tendency for the channel to form as the gate bias is increased. The injection controlling the bipolar current is accompanied by *near* quasi-neutrality ($\Delta n(x) \approx \Delta p(x)$), whereas the channel current, which results due to unipolar injection, does not preserve quasi-neutrality.

The arguments presented above lead to the conclusion that the model for $I_{BJT}$ (especially for transients) is predominantly 1-D. All the same, the gate-controlled (vertical) hole density must also be accounted for in the model. For this reason, the model for $I_{BJT}$ is termed a "quasi-2D" model. Consequently, $I_{BJT}$ in (5.1) is now expressed as

$$I_{BJT} \cong \int\int J_{yBJT}(x, y)dxdy \tag{5.3}$$

where $J_{yBJT}$ is the minority-carrier current density along the lateral direction in the body.

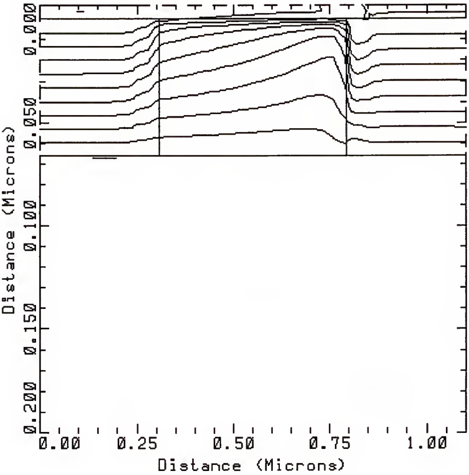


Fig. 5.7 MEDICI-simulated current flowlines of a PD/SOI MOSFET during a transient. The source was pulsed from 1.3 V to -0.2 V. The drain was held at 1.3 V, while the front-gate was held at 0 V. Note that current crowding is forced near the surface, since $V_{GfS}$ is larger compared to the case of Fig. 5.6. The flowlines here are plotted the instant $V_S(t)$ reaches -0.2 V.

### 5.3.2.2 $I_{BJT}$ in Top Portion of SOI Film ($0 \le x \le t_b$)

The analysis of $I_{BJT}$ in the PD/SOI MOSFET is divided into components flowing in the top (possibly depleted) and bottom (neutral) portions of the body, making it consistent with the existing model formulation for a retrograded channel [Suh95]. The bipolar gain in the top portion tends to be larger as the doping in that region is smaller. First, we express the low-injection (electron) current density in the top portion of the film, along the y-direction, as

$$J_{nLTF}(x) = qD_n\frac{\partial}{\partial y}n(x, y) + qn(x, y)\mu_n E_y(x, y) \tag{5.4}$$

where the suffix nLTF stands for electron, low-injection, top-portion, and forward-mode ($V_{BS} > V_{BD}$), respectively. All other terms have their usual meaning. The lateral field $E_y(x,y)$ can be obtained from the condition that the majority carriers (holes in the body) are approximately in detailed balance [Mul85], i.e.,

$$J_{pLTF}(x) = -qD_p\frac{\partial}{\partial y}p(x, y) + qp(x, y)\mu_p E_y(x, y) \cong 0 \quad . \tag{5.5}$$

The validity of (5.5) has been confirmed by 2D MEDICI simulations. From (5.5) and the Einstein relationship [Mul85] we can express the field as

$$E_y(x, y) \cong \frac{kT}{q}\frac{1}{p(x, y)}\frac{\partial}{\partial y}(p(x, y)) \quad . \tag{5.6}$$

Using (5.6) in (5.4), and rearranging, we get

$$J_{nLTF}(x)p(x, y)dy = qD_n d(n(x, y)p(x, y)) \quad . \tag{5.7}$$

Integrating (5.7) between $y = 0$ (body-source junction) and $y = L_{BJT(T)}$ (body-drain junction), and using the fact that $n(x,y = 0)p(x,y = 0)=n_i^2\exp(V_{BS}/V_T)$ and $n(x,y = L_{BJT(T)})p(x,y = L_{BJT(T)}) \approx 0$, we obtain

$$J_{nLTF}(x) = -\frac{qD_n n_i^2 \exp\left(\frac{V_{BS}}{V_T}\right)}{\int_0^{L_{BJT(T)}} p(x, y)dy} \quad . \tag{5.8}$$

We have implicitly assumed here that the pn product is uniform along the x direction at $y = 0$ and $y = L_{BJT(T)}$. (This tends to be true for reasons cited in the previous chapter regarding Fig. 4.8.) $L_{BJT(T)}$ is the length of the quasi-neutral "body" in the top portion of the film along which the carriers flow. It is defined as

$$L_{BJT(T)} = L_{eff} - D_{SL}(V_{BS}) - D_{DL}(V_{BD}) \tag{5.9}$$

where $L_{eff}$ is the electrical channel length of the MOSFET, and $D_{SL}(V_{BS})$, and $D_{DL}(V_{BD})$ are bias-dependent lengths that account for "base-width modulation" [Mul85] in the top portion. The voltage dependences of $D_{SL}$ and $D_{DL}$ are defined based on the depletion approximation [Mul85].

Now, the integral in the denominator of (5.8) can be approximated under low-injection conditions to be

$$\int_0^{L_{BJT(T)}} p(x, y)dy \cong p(x)L_{BJT(T)} \tag{5.10}$$

where p(x) is the gate-controlled hole density at $y = 0$, which varies along the vertical direction. Substituting (5.10) in (5.8) yields

$$J_{nLTF}(x) \cong -\frac{qD_n n_i^2 \exp\left(\frac{V_{BS}}{V_T}\right)}{p(x)L_{BJT(T)}} \quad . \tag{5.11}$$

Note that p(x) controls the Gummel number in the body of the SOI MOSFET. Neglecting Fermi-Dirac statistics, and using the Boltzmann approximation for carrier distribution in the body, we can express p(x) in the top portion of the film to be

$$p(x) \cong N_{BL} \exp\left(-\frac{(\psi(x) - V_{BS})}{V_T}\right) \tag{5.12}$$

where $N_{BL}$ is the body doping in the low-doped part of the hi-lo junction, and ($\psi(x)$-$V_{BS}$) is the effective band bending between a point x in the top portion of the film and the neutral body, as indicated in Fig. 5.8(a). The band bending varies from ($\psi_{sf}$-$V_{BS}$) at the surface to 0 at $x = t_b$; $\psi_{sf}$ is the surface potential controlled by the gate. Since $\psi(x)$ is obtained from (1-D) MOS theory, $p(\psi(x))$ is more appropriately termed as $p^{MOS}(x)$. This definition can be used to distinguish between MOS- and bipolar-controlled charge, as well as define the condition for low injection.

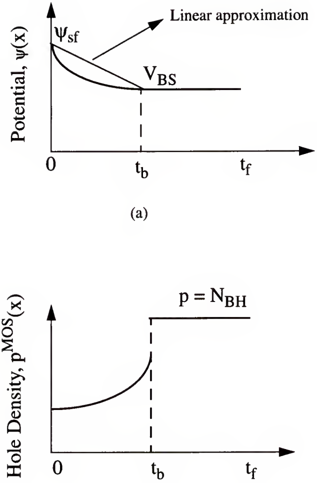
The condition for low injection now is

$$\Delta p(x) \cong \Delta n(x) \ll p^{MOS}(x) \quad . \tag{5.13}$$

To completely describe $p^{MOS}(x)$, we need the potential distribution in the body. In this regard, we can adequately approximate the potential distribution to be linear as illustrated in Fig. 5.8(a):

$$\psi(x) \cong \psi_{sf} - \frac{(\psi_{sf} - V_{BS})}{t_b} x \quad . \tag{5.14}$$

Note that $\psi_{sf}$ (at the source) can vary from $V_{BS}$ in accumulation ($V_{GfB} \leq V_{FB}$) to $\psi_{sfS}$ [Suh95] in strong inversion ($V_{GfS} > V_{TS}$). To ensure its smooth transition across the various boundaries, $\psi_{sf}$ is obtained by interpolation. Consistent with the level of approximation in (5.14), $\psi_{sf}$ can be expressed as



(a)

(b)

Fig. 5.8 Potential distribution $\psi(x)$ in the vertical direction, and the corresponding hole density $p^{MOS}(x)$ in a PD/SOI MOSFET, for the assumed hi-lo junction doping profile.

$$\psi_{sf} = \psi_{sfS} - \frac{(\psi_{sfS} - V_{BS})}{1 + \exp\left(\frac{V_{GfS} - V_{ref}}{\Delta V}\right)} \tag{5.15}$$

where $V_{ref}$ is the reference voltage given by $(V_{FB}+\overline{V}_{BS}+V_{TS})/2$, $\overline{V}_{BS}$ is an average value of $V_{BS}$ that defines a dynamic flatband voltage, and $\Delta V$ defines the slope of the transition of $\psi_{sf}$ between $V_{FB}$ and $V_{TS}$. The corresponding $p^{MOS}(x)$ is shown in Fig. 5.8(b). Equations (5.11)-(5.15) completely describe the low-injection, electron current density in the top portion, including the condition for low injection.

The high-injection electron current density is written from standard analysis [Mul85] as

$$J_{nHF} \cong -\frac{q2D_n n_i \exp\left(\frac{V_{BS}}{2V_T}\right)}{L_{BJT(T)}} \quad , \tag{5.16}$$

which is applicable because the injected carriers screen the MOS-defined potential $\psi(x)$ and negate the sensitivity to the gate voltage. The net current density for any given injection level in the top portion is now given by a weighted sum [Jeo89] as

$$J_{nTF}(x) \cong \frac{J_{nLTF}(x) J_{nH}}{(J_{nLTF}(x) + J_{nH})} \quad , \tag{5.17}$$

which (smoothly) covers intermediate as well low- and high-injection levels. Substituting (5.11) and (5.16) in (5.17), and rearranging yields

$$J_{nTF}(x) \cong -\frac{q2D_n n_i^2 \exp\left(\frac{V_{BS}}{2V_T}\right)}{L_{BJT(T)}} \left[\frac{1}{2p^{MOS}(x) + n_i \exp\left(\frac{V_{BS}}{2V_T}\right)}\right] \quad . \tag{5.18}$$

Note that (5.18) collapses to (5.11) or (5.16) asymptotically depending on the injection level defined by (5.13).

The total bipolar current in the top portion is now obtained by integrating (5.18) between x = 0 and x = $t_b$:

$$I_{BJT(TF)} = -W\int_0^{t_b} J_{nT}(x)dx \quad . \tag{5.19}$$

Using (5.12) and (5.18) in (5.19) and carrying out the integration gives

$$I_{BJT(TF)} = W\frac{2qD_n}{L_{BJT(T)}}n_i^2\left[\frac{1}{p_H a_f}\log\left\{\left(\frac{t2-1}{t1-1}\right)\left(\frac{t1}{t2}\right)\right\}\right]\exp\left(\frac{V_{BS}}{V_T}\right) \quad ; \tag{5.20}$$

where $p_H = n_i\exp(V_{BS}/2/V_T)$, $a_f = [(\psi_{sf}-V_{BS})/V_T/t_b]$, $t2 = 1+(N_{BL}/p_H)$, and $t1 = 1+(p^{MOS}(x = 0)/p_H)$.

Equation (5.20) defines the bipolar current in the top portion for forward mode. In the reverse mode, although $V_{DS} > 0$ causes asymmetry the current is similarly expressed as

$$I_{BJT(TR)} = W\frac{2qD_n}{L_{BJT(T)}}n_i^2\left[\frac{1}{p_H a_f}\log\left\{\left(\frac{t2-1}{t1-1}\right)\left(\frac{t1}{t2}\right)\right\}\right]\exp\left(\frac{V_{BD}}{V_T}\right) \quad . \tag{5.21}$$

Note that we have neglected the $V_{DS}$ dependence of the term in the square brackets. The reason for doing this is related to numerical stability. If the exact dependence were included in (5.21), the term inside the brackets would not behave well for large negative voltages. To avoid this instability, we set this term in (5.21) to be the same as in (5.20). This is reasonable since $V_{BS}$ in the main model routine in SOISPICE is always larger than $V_{BD}$, i.e, $V_{DS} > 0$. Further, typically, the reverse mode BJT current in (5.21) is orders of magnitude smaller than that in forward mode in (5.20). For cases where the reverse-mode current is comparable to that in forward mode (such as near saturation where $V_{BS}$ and $V_{BD}$ are nearly equal), (5.21) approaches (5.20).

The total current in the top portion for both modes is then simply given by

$$I_{BJT(T)} = I_{BJT(TF)} - I_{BJT(TR)} \quad . \tag{5.22}$$

### 5.3.2.3 $I_{BJT}$ in Bottom Portion of SOI Film ($t_b \le x \le t_f - t_b$)

The bottom portion of the film, by definition, is always quasi neutral. Hence, the analysis of the bipolar current is straightforward. The low-injection, forward mode current in the bottom portion has the familiar form:

$$I_{BJT(LBF)} = \frac{qW(t_f - t_b)D_n n_i^2 \exp\left(\frac{V_{BS}}{V_T}\right)}{N_{BH}L_{BJT(B)}} \tag{5.23}$$

where $L_{BJT(B)}$ is the length of the quasi-neutral body in the bottom portion of the film, and $N_{BH}$ is the body doping in the heavily doped part of the hi-lo junction. The equation for $L_{BJT(B)}$ is similar to (5.9) except that the doping dependence (implicit in $D_{SL}$ and $D_{DL}$) would be on $N_{BH}$ here. Also, if a halo is present in the device structure [Suh95], the Gummel number ($N_{BH}L_{BJT(B)}$) is replaced by ($N_{BH}L_{BJT(B)}+N_{HALO}L_{LDS}$). The high-injection current is

$$I_{BJT(HBF)} = \frac{qW(t_f - t_b)2D_n n_i \exp\left(\frac{V_{BS}}{2V_T}\right)}{L_{BJT(B)}} \quad . \tag{5.24}$$

The total bipolar current in the bottom portion (forward mode) is once again obtained as a weighted sum,

$$I_{BJT(BF)} = \frac{I_{BJT(LBF)} I_{BJT(HBF)}}{I_{BJT(LBF)} + I_{BJT(HBF)}} \quad , \tag{5.25}$$

while the total bipolar current in the bottom portion for both modes is written as

$$I_{BJT(B)} = I_{BJT(BF)} - I_{BJT(BR)} \quad . \tag{5.26}$$

### 5.3.2.4 Total $I_{BJT}$ in the SOI Film

The total bipolar current in the SOI film can now be written as the sum of (5.22) and (5.26):

$$I_{BJT} = I_{BJT(T)} + I_{BJT(B)} \quad . \tag{5.27}$$

Equation (5.27) describes the bipolar current for all injection levels, in the top and bottom portions, and is valid for forward and reverse modes of operation.

### 5.3.3 Charge Modeling

In order to model the transient charge dynamics, the bipolar charges associated with each of the terminals must be properly accounted for. Then, the dynamics is modeled using the quasi-static approximation. There are two main components of stored bipolar charge in the SOI MOSFET:

(i) Minority (electrons) carriers stored in a (p-type) body;

(ii) Minority (holes) carriers stored in the (n-type) source.

### 5.3.3.1 Top Portion of the Body ($o \leq x \leq t_b$)

We first consider the minority carriers injected (and subsequently stored) in the top-portion of the body. This component of (excess) charge is simply given by

$$Q_{n(TF)} = Wq\int_0^{t_b}\int_0^{L_{BJT(T)}} \Delta n_{TF}(x, y)dxdy \quad . \tag{5.28}$$

Assuming a linear distribution of electrons in the body (p-type) for all injection levels, we can express $\Delta n_{TF}(x,y)$ as

$$\Delta n_{TF}(x, y) \cong \Delta n_{TF}(x)\left(1 - \frac{y}{L_{BJT(T)}}\right) \quad . \tag{5.29}$$

Substituting (5.29) in (5.28) and evaluating the inner integral gives

$$Q_{n(TF)} \cong \frac{WqL_{BJT(T)}}{2}\int_0^{t_b} \Delta n_{TF}(x)dx \quad . \tag{5.30}$$

In the above equation, $\Delta n_{TF}(x)$ is given by a weighted sum analogous to (5.17):

$$\Delta n_{TF}(x) \cong \frac{\Delta n_{LTF}(x)n_H}{\Delta n_{LTF}(x) + n_H} \tag{5.31}$$

where

$$\Delta n_{LTF}(x) \cong \frac{n_i^2}{p^{MOS}(x)}\left(\exp\left(\frac{V_{BS}}{V_T}\right) - 1\right) \quad , \tag{5.32}$$

and $n_H = n_i\exp(V_{BS}/2/V_T)$. Using (5.31) and (5.32) in (5.30) and carrying out the integration yields the total charge stored in the top-portion of the body in the forward mode:

$$Q_{n(TF)} \cong \frac{WqL_{BJT(T)}}{2}\left[\frac{1}{a_f}\log\left\{\left(\frac{s2-f1}{s1-f1}\right)\left(\frac{s1}{s2}\right)\right\}\right]p_H \tag{5.33}$$

where $f1 = \exp(V_{BS}/V_T)$, $f2 = p^{MOS}(x{=}0)\exp(V_{BS}/2/V_T)/n_i$, $s1 = f1+f2$, and $s2 = f1+f2\exp(a_f t_b)$; $p_H$ and $a_f$ have been defined previously.

In the reverse mode the stored charge is given by

$$Q_{n(TR)} \cong \frac{WqL_{BJT(T)}}{2}\left[\frac{1}{a_f}\log\left\{\left(\frac{s2-f1}{s1-f1}\right)\left(\frac{s1}{s2}\right)\right\}\right]p_R \tag{5.34}$$

where $p_R = n_i\exp(V_{BD}/2/V_T)$. Once again for numerical reasons outlined regarding (5.20) and (5.21) in Sec. 5.3.2.2, the terms in the square brackets in (5.33) and (5.34) are set to be equal.

### 5.3.3.2 Bottom Portion of the Body ($t_b \leq x \leq t_f - t_b$)

In the (quasi-neutral) bottom portion, we can write the total stored charge in the forward mode as a weighted sum of the low- and high-injection charge components as

$$Q_{n(BF)} \cong \frac{WqL_{BJT(B)}}{2}(t_f - t_b)\left(\left(\frac{\frac{n_i^2}{N_{BH}}\exp\left(\frac{V_{BS}}{V_T}\right)p_H}{\frac{n_i^2}{N_{BH}}\exp\left(\frac{V_{BS}}{V_T}\right)+p_H}\right)-\frac{n_i^2}{N_{BH}}\right), \tag{5.35}$$

while the reverse-mode stored charge $Q_{n(BR)}$ can be obtained by replacing $V_{BS}$ with $V_{BD}$ in (5.35).

### 5.3.3.3 Quasi-Neutral Source

In the source, the charge storage (holes in n-type source) can be two-dimensional, depending on the device structure. Also, the effects of heavy doping in the source [Fos81] must be accounted for. The stored charge in the source is given by

$$Q_{p(F)} \cong \frac{WqL_{DIFF}}{2} t_f \frac{n_i^2}{N_{DS(eff))}} \left( \exp\left( \frac{V_{BS}}{V_T} \right) - 1 \right) \quad . \tag{5.36}$$

In the above equation, $L_{DIFF}$ is an effective 2-D diffusion length in the source, and $N_{DS(eff)}$ is the effective (constant, but temperature-dependent) doping in the source that accounts for heavy-doping effects such as Fermi-Dirac statistics and energy-gap narrowing [Fos81]. In the reverse mode, we can obtain $Q_{p(R)}$ by simply replacing $V_{BS}$ with $V_{BD}$.

### 5.3.3.4 Charge Allocation

The bipolar stored charges characterized above must be allocated properly to the appropriate terminals. From physical insight, we can write,

$$Q_S = Q_S - Q_{n(TF)} - Q_{p(F)} \quad , \tag{5.37}$$

$$Q_D = Q_D - Q_{n(TR)} - Q_{p(R)} \quad , \tag{5.38}$$

and

$$Q_B = Q_B + Q_{n(TF)} + Q_{p(F)} + Q_{n(TR)} + Q_{p(R)} . \tag{5.39}$$

### 5.3.4 Recombination Current

Recombination current (in the body-source junction as well as the quasi-neutral source) is important to account for bipolar-related effects. The present model for recombination current in SOISPICE has a hard-wired term for the “effective” surface recombination velocity $S_{EFF}$. Since $S_{EFF}$ can vary depending on the processing conditions, as well as on fundamental lifetimes (e.g., Auger lifetime), it is important for the user to have this as a model parameter. With the above insight, we now rewrite the recombination current in [Suh95] as

$$I_R(V_{BS}) = WJ_{RO}\exp\left(\frac{V_{BS}}{MV_T}\right) + Wt_f\frac{qn_i^2}{N_{DS(eff)}}S_{EFF}\exp\left(\frac{V_{BS}}{V_T}\right) \quad , \quad (5.40)$$

adding $S_{EFF}$ as a new model parameter.

### 5.3.5 Parasitic BJT Modeling for the FD/SOI MOSFET

Even though the transient parasitic BJT effect in the FD/SOI MOSFET tends to be less significant than for the PD/SOI MOSFET (primarily due to a relatively weak Gf-B-S capacitive coupling under FD mode of operation), it can still be important when $V_{GfB} < V_{FB}$. To study this effect in the FD/SOI MOSFET, a reliable parasitic bipolar model is needed. Based on the analysis in the top portion for the PD/SOI MOSFET (Sections 5.3.2.2 and 5.3.3.1) it is possible to extend the parasitic model for the FD/SOI MOSFET, but with certain modifications.

The bipolar current for the FD/SOI MOSFET is separated into that controlled by the front and back gates. The analysis for the front gate is similar to that for the PD/SOI MOS-

FET in Sec. 5.3.2.2, but with $V_{BS}$ in (5.14) replaced by the back-surface potential $\psi_{sb}$. The model for $\psi_{sf}$ is the same as that in (5.15). The analogous model for $\psi_{sb}$ is similar to (5.15), but with $V_{GfS}$, $\psi_{sfS}$, and $V_{TS}$, respectively, replaced by $V_{GbS}$, $2\phi_b$ ( = 2[ kTlog($N_{BODY}/n_i$)]), and $V_{TWB}$ ($V_{GbS}$ for $\psi_{sb} = 2\phi_b$). The charge modeling (front and back gate) for the FD/SOI MOSFET is analogous to that for the PD/SOI MOSFET described in Sec. 5.3.3.1, including the model for $\psi_{sb}$.

### 5.3.6 Significance of BiMOS Modeling

The bipolar model developed above is coupled directly to the MOSFET model not only due to the dependence of the hole density $p^{MOS}(x)$ on the gate-bias, but also, and more importantly, due to the fact that both are based on one *single* set of (physical) parameters. This will make the (physics-based) parameter evaluation straightforward, as will be described in the following chapter. This is in contrast to use of an (empirical) sub-circuit representation of the SOI MOSFET, where two (BJT and MOSFET) sets of parameters will be needed. The ensuing parameter evaluation methodology will not only be tedious, but will also be inadequate due to the empirical representation.

## 5.4 Model Implementation

The bipolar model has been implemented directly in the SOISPICE [Fos95]. Since all currents and charges discussed in the previous section have analytical and closed-form expressions, the implementation process was straightforward. An existing (empirical) model parameter, VJMIN was removed since the new modeling made it redundant. A new model parameter SEFF (described in Sec. 5.3.4) was added to the PD model. Also, FVBJT is not used in the BiMOS models, as described, but it may be used to empirically account for breakdown in strong inversion.

## 5.5 Model Verification and Discussion

### 5.5.1 Introduction

The BiMOS model developed here is predominantly for use in transient applications, even though breakdown (or latch) in DC may also be predicted. Hence, the modeling of the bipolar transport current as well as the stored charges will have to be verified based on transient simulations and measured data. We first use transient simulations of MEDICI [Med94] to comprehensively verify the model. As described in the following chapter, the model is also verified with measured transient data.

### 5.5.2 Verification with 2-D MEDICI Simulations

A representative device structure was first selected based on a generic (n-channel) PD/SOI MOSFET [A. Wei, MIT, Private Communication]. The MEDICI input deck was then generated based on this device. Care was taken to define realistic physical parameters for the models in MEDICI. For example, the carrier lifetime model in the source region was modified so that for the specified doping concentration ($N_{DS} = 5\text{x}10^{19}\ \text{cm}^{-3}$) the dominant lifetime was due to the band-band Auger recombination process. Use of a non-physical lifetime model can not only lead to wrong recombination rates, but will also result in an incorrect accounting of stored charge (or diffusion capacitance) in the source. Other parameters in MEDICI altered from their default values were related to the energy-gap narrowing model. Table 5.1 gives structural information for the simulated generic device.

Table 5.1: DEVICE STRUCTURE INFORMATION

| Name | Description | MEDICI | SOISPICE |
|---|---|---|---|
| LEFF | Electrical channel length | 0.484 μm | 0.484 μm |
| TOXF | Front-oxide thickness | 6.9 nm | 6.9 nm |
| TOXB | Back-oxide thickness | 360 nm | 360 nm |
| TF | Silicon film thickness | 66 nm | 66 nm |
| NBL | Low body doping density | $6.25\text{x}10^{17}\text{cm}^{-3}$ | $6.25\text{x}10^{17}\text{cm}^{-3}$ |
| NBH | High body doping density | $6.25\text{x}10^{17}\text{cm}^{-3}$ | $6.25\text{x}10^{17}\text{cm}^{-3}$ |
| NDS | Source/Drain doping density | $5\text{x}10^{19}\text{cm}^{-3}$ | $5\text{x}10^{19}\text{cm}^{-3}$ |
| RS/RD | Source/Drain contact resistance | 300 ohm-μm | 300 ohm-μm |

As shown in Table 5.1, the SOISPICE NFD model parameters related to device structure (e.g., $N_{BL}$, $L_{eff}$) were directly adapted from the MEDICI-defined structure. A few (physical) parameters had to be evaluated from DC I-V characteristics (although not rigorously here), the process of which is comprehensively described in the following chapter. Figure 5.9 shows SOISPICE-predicted $I_{DS}$-$V_{Gfs}$ characteristics compared with MEDICI. Note that the subthreshold slope at low $V_{DS}$, as well as the kink at high $V_{DS}$ are predicted well. The discrepancy between SOISPICE and MEDICI is mainly in the moderate-inversion region. However, since parameter evaluation is not done in this region, the set of model parameters obtained is physically representative. Table 5.2 lists the parameters in SOISPICE evaluated from DC $I_{DS}$-$V_{Gfs}$ characteristics. Two other parameters, LDIFF, and SEFF, related to the bipolar model, were also evaluated directly from structure. Since the source/drain contacts in MEDICI were placed on the sides, and the distribution of holes in the source (predicted by MEDICI) was 1-D and linear (transit time << recombination lifetime), LDIFF in (5.36) is approximately $L_S/2$ ($L_S$ is the distance from the source-body junction to the contact in MEDICI). Further, the linear distribution of holes also implies that SEFF in (5.40) can be estimated to be $D_p/L_S$ [Fos81], where $D_p$ is the diffusivity of holes in the source.

Figure 5.10 compares SOISPICE and MEDICI predictions of low-voltage transient leakage current, i.e., $I_D(t) \sim I_{BJT}(t)$, in the pass-transistor circuit [Pel95] shown in Fig. 5.2 for two different (effective) channel lengths ($L_{eff}$). The supply voltage $V_{DD}$ was set at 1.5 V, while the fall time $t_f$ was 4.5 ns. As can be seen from Fig. 5.10, the bipolar current increases as $L_{eff}$ is scaled down, but only relatively weakly. The new BiMOS model, in accord with MEDICI, predicts this weak dependence of the transient current on $L_{eff}$, even though $I_{BJT} \propto 1/L_{eff}$. This is due to the Gf-B-S capacitive coupling in Fig. 5.3, which controls $V_{BS}(t)$. As L is scaled, the Gf-B capacitance ($C_{of} \propto L$) is reduced proportionally, whereas the B-S diffusion capacitance ($C_{diff}$) is not. In fact the source component of the B-S diffusion capacitance is independent of $L_{eff}$ as implied by stored charge in the source in (5.36). The Gf-B capacitive coupling is hence reduced relative to the B-S coupling, and $V_{BS}(t)$ tends to be suppressed in the smaller device. Indeed, depending on the device structure, $I_{BJT}(t)$ can actually decrease as L is scaled because of the relative capacitive-coupling dependence on L. This is in accord with recently measured data [Ass96]. A point worth noting is that the transient current plotted in Fig. 5.10 is that flowing through the drain. This is the component of interest with regard to leakage in circuits. In the source, there are additional components; e.g., a displacement current flowing from the gate due to

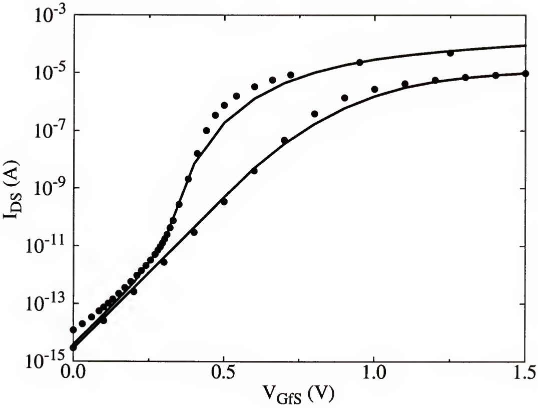


Fig. 5.9 Model calibration (solid curves) to MEDICI $I_{DS}$-$V_{GfS}$ characteristics (points) at low and high ($V_{DS}$ = 0.1 V, 1.5 V). Model parameters tuned based on the characteristics here are listed in Table 5.2 below.

Table 5.2: SOISPICE PARAMETERS EVALUATED FROM I-V CHARACTERISTICS

| Parameter | Description | Value |
|---|---|---|
| TB | Effective film thickness | 37 nm |
| JRO | Junction recombination current coefficient | $2\text{x}10^{-10}$ A/m |
| M | Junction non-ideality factor | 1.8 |

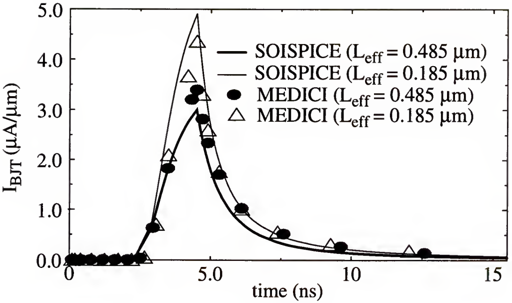


Fig. 5.10 SOISPICE- and MEDICI-predicted transient drain current (= $I_{BJT}(t)$) for two different channel lengths. For all simulations, the PD/SOI MOSFET had front-oxide thickness $t_{of}$ = 6.9 nm, SOI film thickness $t_f$ = 66 nm, back-oxide thickness $t_{ob}$ = 360 nm, and (uniform) channel doping density $N_{BL} = 6.25\text{x}10^{17}$ cm$^{-3}$; the supply voltage $V_{DD}$ was 1.5 V, and the fall rate of the source-voltage pulse $V_S(t)$ was 1.5V/4.5 ns.

the $V_S(t)$ pulse, constitutes a charging current in the source. Also, in general, $I_D(t)$ could include $I_{CH}$ and/or displacement currents between the body-drain junction, depending on the threshold voltage as well as the fall rate of $V_S(t)$. If the bipolar current is the dominant component, the current would decay rather rapidly ($I_{BJT}(t) \propto \exp(V_{BS}(t)/V_T)$ as implied by decreasing $V_{BS}(t)$ after $V_S(t)$ is removed. However, if the channel current is the dominant leakage component, the transient decay would be much slower, since $I_{CH}(t) \propto \exp(\alpha V_{BS}(t)/(1+\alpha)/V_T)$ in this region, and $\alpha$ in PD/SOI MOSFETs is typically about 0.5 [Suh95]. Hence, the rate of decay of the transient drain current is an indication of the nature of the leakage. Typically in devices with high threshold voltage (e.g., in DRAMs), the dominant leakage current tends to be due to the bipolar effect. In devices with a relatively low threshold, both may be important. In Fig. 5.10 the leakage current is predominantly due to the bipolar effect, i.e., $I_D(t) \approx I_{BJT}(t)$.

### 5.5.3 $I_{BJT}$ Dependence on Fall Rate: Significance of Diffusion Capacitance

The model is further verified with MEDICI in Fig. 5.11, where the fall rate of $V_S(t)$ in Fig. 5.2 (or equivalently $\Delta V_S/t_f$) is increased. Both SOISPICE and MEDICI show that the magnitude of the transient current increases, but the increase ultimately saturates. To understand the reason for this saturation, it is instructive to consider the nodal equation in the body (at B') when the source-voltage pulse is falling ($0 \leq t \leq t_f$):

$$\frac{dQ_B}{dt} \cong -I_R(V_{BS}) \quad . \qquad (5.41)$$

Now, using the quasi-static approximation for the body-charging current $dQ_B/dt$, while simultaneously expressing $Q_B$ from charge neutrality, we get

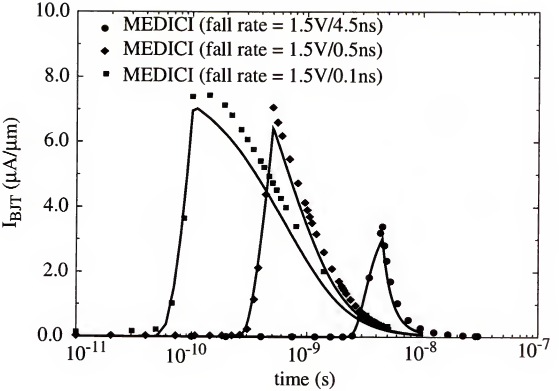


Fig. 5.11 SOISPICE (solid curves)- and MEDICI-predicted $I_{BJT}(t)$ versus time (log scale) for varying $V_S(t)$ fall rates for the $L_{eff} = 0.485$ μm device. Note that the peak $I_{BJT}$ tends to increase with increasing fall rate, but ultimately saturates due to the $V_{BS}$-enhanced diffusion capacitance that limits any further increase in $V_{BS}(t)$. The initial decay rate of $I_{BJT}(t)$ is nearly independent of the fall rate as dictated by the ratio of recombination current to diffusion capacitance.

$$-\frac{d(Q_{Gf}+Q_S)}{dV_{GfS}}\frac{dV_{GfS}}{dt}-\frac{d(Q_{Gf}+Q_S)}{dV_{BS}}\frac{dV_{BS}}{dt}\cong -I_R(V_{BS}) \quad . \tag{5.42}$$

Note that the dominant components of terminal charges for this transient are $Q_{Gf}$, $Q_S$, and $Q_B$. Also in the derivation of (5.42), the charging current components in the drain, (i.e., all components related to $dV_{DS}/dt$) are neglected. Further, from the charge modeling we can also approximate $dQ_{GfS}/dV_{GfS} \approx C_{of}$ and $dQ_{GfS}/dV_{BS} \approx -C_{of}$ for this transient. Using these approximations, expressing $dV_{GfS}/dt$ as $\Delta V_S/t_f$ (> 0), and rearranging (5.42) yields

$$\frac{dV_{BS}}{dt}\cong\frac{C_{of}\frac{\Delta V_S}{t_f}-I_R(V_{BS})}{C_{of}-\frac{\partial Q_S}{\partial V_{BS}}}=\frac{C_{of}\frac{\Delta V_S}{t_f}-I_R(V_{BS})}{C_{of}+C_{diff}(V_{BS})} \quad . \tag{5.43}$$

Equation (5.43) provides insight on how the $V_{BS}(t)$-dependent diffusion capacitance $C_{diff}(V_{BS})$ associated with the B-S junction limits $V_{BS}(t)$. It is worthwhile to note that as the fall rate is increased, the diffusion capacitance tends to become more important than recombination insofar as limiting $V_{BS}(t)$ and, consequently, the peak $I_{BJT}(t)$. Mathematically, this implies $C_{of}\Delta V_S/t_f >> I_R(V_{BS})$ in (5.43). Physically, it means that the recombination rate is much smaller than the body-charging rate (as implied by the falling source-voltage pulse). Consequently, injected (excess) carriers cannot be effectively removed in the short time that the pulse is falling. From (5.43), the limiting $V_{BS}$ (independent of the fall rate) due to diffusion capacitance can be estimated to be

$$V_{BS}^{max}\cong V_T\log\left(\frac{C_{of}\Delta V_S}{C_{diff0}V_T}\right) \quad , \tag{5.44}$$

where $C_{diff0}$ is the coefficient of the diffusion capacitance ($C_{diff} \approx C_{diff0}\exp(V_{BS}/V_T)$), and is implied by (stored) the charges in (5.33) and (5.36). Note however that after the fall of the source-voltage pulse ($t > t_f$), the body nodal equation dictates

$$\frac{dV_{BS}}{dt} \cong \frac{-I_R(V_{BS})}{(C_{of} + C_{diff}(V_{BS}))} \quad . \tag{5.45}$$

Hence, after the fall of the pulse, we can see clearly that recombination becomes important. The effect of diffusion capacitance in this regime is to slow the transient decay of $I_{BJT}(t)$. An interesting fact evidenced in Fig. 5.11 concerns the rise and decay time constants of the $I_{BJT}(t)$ pulse. The rise time of $I_{BJT}(t)$ is predominantly controlled by the input pulse, as implied by (5.43). On the other hand, the initial decay (or fall) time constant is nearly independent of the input pulse characteristics. From (5.45) the initial decay time constant can be roughly estimated to be

$$\tau_{decay(init)} \cong \frac{C_{diff0}}{I_{R0}} V_T \tag{5.46}$$

where $I_{R0}$ is the coefficient of the second term in (5.40). (After the constant initial decay rate, the secondary decay rate involves complex $V_{BS}$-dependent time constants due to nonlinear recombination rates.) Now, we can use the insight gained from (5.43) and (5.45) to identify ways of controlling $I_{BJT}(t)$.

## 5.6 Design Insight

The key to control $I_{BJT}(t)$ is to suppress $V_{BS}(t)$. Insight derived from our BiMOS modeling suggests that control of $V_{BS}(t)$ might be effected by *designing for capacitance* as well as recombination. The latter has been aimed at reducing the emitter injection efficiency of the parasitic BJT, for example with a SiGe source/drain [Yos95]. By the former design criterion, we mean enhancing the bipolar charge storage, i.e., diffusion capacitance, to control the BiMOS capacitive coupling so as to suppress $V_{BS}(t)$. This will not undermine SOI CMOS speed performance since the diffusion capacitance obtains only at forward-biased junctions. It can be effected by the SiGe source/drain (if indeed heterojunctions are formed by the process [Yos95]). SOISPICE simulations of a SiGe source/drain pass transistor were done, assuming a Ge-induced bandgap reduction of 0.1 eV [Yos95]. Fig. 5.12 compares the predicted $I_{BJT}(t)$ with that obtained for the Si source/drain counterpart. The transient leakage current is suppressed dramatically, due in large part to the added diffusion capacitance of the SiGe source/drain as indicated by the controlled simulation results in Fig. 5.13. Note that the diffusion capacitance limits the peak $I_{BJT}(t)$ (critical in SRAM), but that the added recombination current is important as well since it quickens the decay of the transient current (critical in DRAM). These results indicate then that the benefit of designing for capacitance will depend on the particular circuit application.

## 5.7 Summary and Conclusions

In this chapter, it has been shown that the transient parasitic bipolar effect can be important in scaled PD/SOI MOSFETs even at low voltages well below the drain-source breakdown. The transient effect, which occurs due to dynamic charging of the floating body in the MOSFET, can cause loss of stored charge in DRAMs and lead to “upsets” in

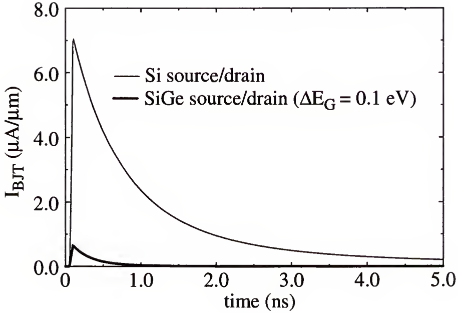


Fig. 5.12 SOISPICE-predicted reduction in $I_{BJT}(t)$ afforded by a SiGe source/drain for the $L_{eff} = 0.485$ μm device. The $V_S(t)$ fall rate was 1.5V/0.1 ns.

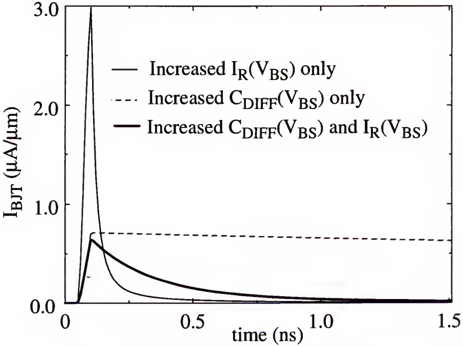


Fig. 5.13 Controlled SOISPICE simulation results showing relative effects of increased recombination current and diffusion capacitance on reduction of $I_{BJT}(t)$ for the SiGe-source/drain device corresponding to Fig. 5.12. Note how the diffusion capacitance significantly reduces the peak value, whereas the recombination current quickens the decay.

SRAMs. Further, soft error rate (due to an alpha particle) in SOI MOSFETs is also amplified due to the transient BJT current. To thoroughly assess this effect a quasi-2D, *BiMOS* model, coupling the parasitic BJT to the MOSFET with a single set of parameters, was developed for the NFD (or PD) and FD models in SOISPICE, and was subsequently verified based on 2-D MEDICI simulations. Insight gained from the model was used to propose a new concept for device design to suppress the transient bipolar. In addition to recombination, it was shown that enhancing the stored charge (or diffusion capacitance) can be effective in controlling $I_{BJT}(t)$ as well. The efficacy of increasing diffusion capacitance may depend on the application (i.e., whether peak current or the integrated charge is critical). To properly study this effect, the BiMOS parameters must be evaluated in a physical way. This is the focus of discussion of the following chapter.

# CHAPTER 6
# SYSTEMATIC, PHYSICS-BASED PARAMETER-EVALUATION METHODOLOGY FOR USE WITH SOISPICE

## 6.1 Introduction

SOISPICE [Fos95] has physical, charge-based models for non-fully depleted (NFD) or partially depleted (PD) [Suh95] as well as fully depleted (FD) [Yeh95] SOI MOSFETs. In order to use SOISPICE reliably and efficiently, the model parameters have to be evaluated properly. Since most of the model parameters are based either on the device structure or on the underlying device physics, the resulting parameter-evaluation procedure is relatively straightforward. The key to parameter evaluation here is to recognize that one or more model parameters exhibit a characteristic signature in a given region of the measured current-voltage (I-V) characteristics. Then, from knowledge of device physics in that region, it is possible to systematically isolate parameters of interest. This method of obtaining parameters will highlight the usefulness of physical modeling, for which model parameters can be correlated to the actual process. Further, insight obtained from the procedure can also shed light into device design.

This chapter, then, will first clearly outline a systematic procedure for physics-based parameter evaluation for both FD and PD/SOI MOSFETs, with a detailed description of the constituent steps that lead to the final set of model parameters for a given device. The efficacy of this technique will then be demonstrated by applying it to a wide range of actual FD/ and PD/SOI technologies, given the measured DC I-V characteristics. For the PD/SOI MOSFET, the methodology will be extended to calibrate the new BiMOS model (in transients), which was described in the previous chapter.

## 6.2 General Approach to Parameter Evaluation

First we outline here the general approach to parameter evaluation for application in SOISPICE. As mentioned before, the model parameters will be evaluated mainly from DC measured characteristics. In a given region of operation, one or more parameters tend to exhibit a characteristic signature as governed by the underlying device physics. Hence, the physical modeling can be taken advantage of for purposes of parameter evaluation. An important point to note is that all the parameters are evaluated from I-V data only in regions of low-power, i.e., where self-heating is minimal. Consequently, DC self-heating is not an issue; SOISPICE (with self-heating not accounted for) will be valid in general transient simulation where self-heating effects may not be significant [Su94]. The effects of self-heating tend to be minimized as the supply voltage is scaled, e.g., for low-voltage/ low-power applications. Recent work which suggests use of pulsed I-V data (to avoid self-heating) for parameter evaluation [Jen94] in PD/SOI MOSFETs may not be unambiguous as dynamic floating-body effects [Suh94b, Suh95] can be introduced, leading to erroneous prediction of “steady-state” characteristics.

To start with, an initial set of parameters must be assumed, from processing (technology), or 2-D process simulation, e.g., with SUPREM. Since the SOISPICE models are physical with several structural parameters, this initial evaluation is straightforward and indeed can give very good estimates for the parameter values. The (assumed) initial values for the parameters however need not be known with a great degree of certainty. Once the initial values are obtained, the calibration methodology can be applied in a systematic manner. We will detail the procedure for evaluation for both FD and PD SOI MOSFETs based on DC data, and extend the PD model calibration to include the transient bipolar effect.

## 6.3 Parameter Evaluation for FD/SOI MOSFETs

The basic model formalism for the FD/SOI MOSFET is based on the works of Lim [Lim84] and Veeraraghavan [Vee88b]. Recently, the channel current formalism was extensively modified in weak inversion by Yeh [Yeh95] to account for 2-D fringing fields in the buried oxide, in addition to defining a cubic spline for the moderate-inversion region. A non-local model for impact ionization, described in Chapter 2, has also been added.

The model parameters, along with their description are listed in Table 6.1. Also listed are their typical values for current state-of-the-art FD/SOI technologies. Now, given the technology, **TOXF**, **TOXB**, **TPS**, **TPG**, and **NSUB** are usually well known. Hence, they can be directly specified in the input model card. The *critical* parameters in the table that usually have to be evaluated are **TB, NSB, NBODY, DL**, **GAMMA**, **KAPPA**, **RS/RD**, **UO**, **THETA**, **VSAT**, and **JRO**. If an LDS/LDD is present in the structure, **LLDS/LLDD** and **NLDS** must also be estimated. Some of the other listed parameters are either calculated if defaulted (e.g., **VFBF**), or are simply user-controlled flags (e.g., **ETA**, **LMOD**). Still some other parameters (e.g., **BFACT**) have only a secondary effect on the device

Table 6.1: FD/SOI MODEL PARAMETERS IN SOISPICE

| Name | Description | Typical range of values |
|---|---|---|
| VFBF | Front-gate flatband voltage | Calculated if defaulted |
| VFBB | Back-gate flatband voltage | Calculated if defaulted |
| WKF | Front-gate work function difference | Calculated if defaulted |
| WKB | Back-gate work function difference | Calculated if defaulted |
| NQFF | Front oxide fixed charge | ~ $10^{10}$ $cm^{-2}$ |
| NQFB | Back oxide fixed charge | ~$10^{10}$ -$10^{11}$ $cm^{-2}$ |
| TOXF | Front-gate oxide thickness | 4-10 nm |
| TOXB | Back-gate oxide thickness | 80-400 nm |
| NSUB | Substrate doping density | $10^{15}$-$10^{17}$ $cm^{-3}$ |
| NGATE | Poly gate doping density | ~ $10^{20}$ $cm^{-3}$ |
| NSF | Front surface state charge density | $10^{10}$ $cm^{-2}$ /eV |
| NSB | Back surface state charge density | $10^{10}$-$10^{11}$ $cm^{-2}$ /eV |
| TPG | Type of gate material:<br>+1) opposite to body<br>-1) same as body<br>0) Aluminum | +1 |
| TPS | Type of substrate material:<br>+1) opposite to body<br>-1) same as body | -1 |
| TB | Silicon film thickness | 30-100 nm |
| NBODY | Body (constant) doping density | > $10^{17}$ $cm^{-3}$ |
| CGFBO | Gate-body overlap capacitance | ~ $10^{-10}$ F/m |
| RHOSD | Source/drain sheet resistance | Ohms/sq |

Table 6.1: --(Continued)

| Name | Description | Typical range of values |
|---|---|---|
| UO | Zero-field mobility | 200-600 $cm^2/(V.s)$ (NMOS)<br>70-400 $cm^2/(V.s)$ (PMOS) |
| THETA | Mobility degradation coefficient | $(0.1\text{-}3)\times10^{-6}$ cm/V |
| BFACT | $V_{DS}$-averaging factor for mobility degradation | 0.1-0.5 |
| VSAT | Carrier saturated drift velocity | $(0.5\text{-}1)\times10^{7}$ cm/s |
| ZETA | On/off flag for charge sharing (0 for no charge sharing) | 1 |
| ALPHA | Impact-ionization parameter $\alpha_0$ | $2.45\times10^{6}$ /cm |
| BETA | Impact-ionization parameter $\beta_0$ | $1.92\times10^{6}$ V/cm |
| GAMMA | BOX fringing field weighting factor | 0.3-1.0 |
| TAUO | Carrier life time in the body | $10^{-5}$-$10^{-8}$ s |
| LDS | LDS region length (0 for no LDS) | 0.05-0.2 μm |
| LDD | LDD region length (0 for no LDD) | 0.05-0.2 μm |
| NLDS | LDD/LDS doping density | ~ $10^{18}$ $cm^{-3}$ |
| NDS | Source/drain doping density | > $5\times10^{19}$ $cm^{-3}$ |
| JRO | Source recombination current coefficient | $10^{-15}$-$10^{-17}$ A./m |
| ETA | On/off flag for DICE (0 for no DICE) | 1 |
| LMOD | On/off flag for channel-length modulation | 1 |
| CGFDO | Gate-drain overlap capacitance | ~ $10^{-10}$ F/m |
| CGFSO | Gate-source overlap capacitance | ~ $10^{-10}$ F/m |
| CGFBO | Gate-body overlap capacitance | ~ $10^{-10}$ F/m |
| RHOSD | Source/drain sheet resistance | Ohms/sq |
| RHOB | Body sheet resistance | Ohms/sq |

Table 6.1: --(Continued)

| Name | Description | Typical range of values |
|---|---|---|
| RD | Specific drain parasitic resistance | 300-1000 Ω-μm |
| RS | Specific source parasitic resistance | 300-1000 Ω-μm |
| RB | Body parasitic resistance | $> 10^5$ Ω |
| DL | Channel-length reduction | 0.05-0.2 μm |
| DW | Channel-width reduction | 0.1-0.5 μm |
| KAPPA | BOX fringing field factor | 0.5-1.0 |

characteristics. Hence, parameter evaluation is restricted to only a few structural and physical parameters. We will detail the evaluation process systematically by considering different regions of operation where these key parameters have certain characteristic signatures.

### 6.3.1 Subthreshold Region

In the subthreshold region, the current conduction mechanism in an SOI MOSFET is predominantly by carrier diffusion [Sze81], and can hence be modeled in a rather straightforward manner. The subthreshold slope for a FD/SOI MOSFET predicted by such a model will be nearly ideal at room temperature (i.e., the gate swing is about 60 mV/dec) [Col91]. The current in this region can then be used to obtain information on the SOI film thickness **TB**, the (uniform) body doping **NBODY**, and the lateral source/drain diffusion length **DL**. Recently, however, it was shown that in scaled FD/SOI MOSFETs 2-D fringing fields in the buried oxide can affect the subthreshold characteristics, and therefore they have to be accounted for in the modeling [Yeh95]. Hence, in addition to extracting **TB**, **DL**, and **NBODY**, model parameters pertaining to fringing **GAMMA** and **KAPPA** have to be evaluated too. Another parameter that can influence the subthreshold characteristics is **NSB**, the surface-state density at the back; **NSF** at the front is usually negligibly small ( $< 10^{10}$ cm$^{-2}$/eV).

#### 6.3.1.1 Calibration Based on Subthreshold Slope

Before detailing the parameter-evaluation process in the subthreshold region, it will be useful to establish if **NSB** is significant in the given technology. This will help simplify the

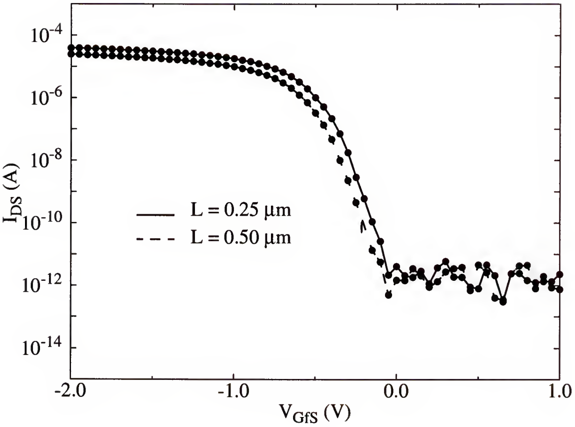


Fig. 6.1 Measured subthreshold characteristics of PMOS FD/SOI MOSFETs at low drain bias ($V_{DS}$ = -0.05 V) for two different L (0.5 μm and 0.25 μm). $S_o$ is about 68 mV/dec and is also nearly independent of L.

Table 6.2: FRINGING PARAMETERS GAMMA AND KAPPA (EXTRACTED FROM MEDICI)

| TOXB (nm) | GAMMA | KAPPA |
|---|---|---|
| ≤50 | 1.0 | 1.0 |
| 100 | 0.7 | 0.9 |
| 200 | 0.5 | 0.7 |
| 350 | 0.3 | 0.5 |

evaluation process considerably. A quick way to identify whether **NSB** is important or not is to examine the subthreshold swing factor $S_o$ at low drain bias for a relatively long-channel device ($L > 0.5$ µm) in that technology. If $S_o$ for this long device is nearly ideal, then we can assume that **NSB** need not be accounted for in the calibration process. However, if $S_o$ is much larger than 60 mV/dec (for this long L), then **NSB** is important, and in fact it can be calibrated from the slope. Note that **NSB** changes $S_o$ from its near-ideal value of $60(1+\alpha)$ to $60(1+\alpha_r)$, where $\alpha_r = C_b r_b C_{ob}/[C_{of}(C_b+r_b C_{ob})]$ with $r_b = 1+q\mathbf{NSB}/C_{ob}$ [Yeh95]; **NSB** low means $r_b \approx 1$ which implies $\alpha_r \approx \alpha$. Hence, the effect of **NSB** is to stretch the $I_{DS}$-$V_{Gfs}$ characteristics in the subthreshold region. For example, Fig. 6.1 shows the measured subthreshold characteristics of a 0.5 µm PMOS FD/SOI MOSFET. The fact that the slope $S_o$ is non-ideal (about 68 mV/dec), and that it is constant for varying L for this technology indicates that **NSB** is important. Once the importance of **NSB** is assessed, then it can either be subsequently evaluated as outlined above, or ignored as the case may be.

Now we can proceed to calibrate **TB**, **DL**, **NBODY**, **GAMMA**, and **KAPPA** for a given device. Normally, **TB** can be defined directly from technology. However, it is possible in certain cases that the film thickness is not uniform over the entire wafer. Consequently, the model parameter **TB** and the actual (variable) SOI film thickness do not have to be necessarily the same, i.e., **TB** should be tuned. If $S_o$ is non-ideal (due to fringing in the buried oxide, and not due to **NSB**), then **TB**, **DL**, and **GAMMA** (**KAPPA** is important only at high $V_{DS}$) can be extracted. A very good initial guess for **GAMMA**, given **TOXB**, can be estimated from Table 6.2. These values for **GAMMA** and **KAPPA** were extracted from 2-D MEDICI simulations for varying **TOXB** [Yeh95]. With this

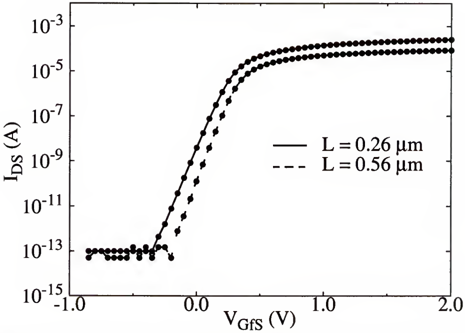


Fig. 6.2 Measured subthreshold characteristics of NMOS FD/SOI MOSFETs at low $V_{DS}$ (= 0.05 V) for different L, those show the effects of fringing.

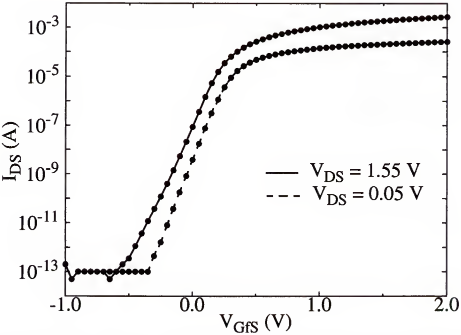


Fig. 6.3 Measured subthreshold characteristics of a 0.26 μm NMOS FD/SOI MOSFET at low and high $V_{DS}$, which shows increased fringing at high $V_{DS}$.

initial value for **GAMMA**, **DL** and **TB** can then be tuned to obtain the right $S_o$. In general, when fringing is important, $S_o$ is most sensitive to **DL**. One way to determine if fringing is important is to examine $S_o$ for different L in a given technology. If $S_o$ increases for scaled L, then fringing is important. (The measured subthreshold characteristics for varying L in Fig. 6.1 do not exhibit fringing, whereas those in Fig. 6.2 clearly do.) Another way to ascertain if fringing is significant is to check the subthreshold swing at high $V_{DS}$, S, relative to $S_o$. The measured subthreshold characteristics for a 0.26 μm device in Fig. 6.3 at high $V_{DS}$ shows degradation due to increased fringing: $S > S_o$. As mentioned earlier, the parameter **KAPPA** is responsible for the increased fringing at high $V_{DS}$, and hence can be obtained from tuning the slope S in this region. (Again, a good initial guess for **KAPPA** can be obtained from Table 6.2. In some cases no further tuning of these fringing parameters may be necessary.) **NBODY** usually has only a secondary effect on $S_o$ and S.

#### 6.3.1.2 Calibration Based on Subthreshold Current

The current in this region, which depends on the gate-controlled body charge (QB ∝ **NBODY*TB**), can now be used to calibrate **NBODY**. If necessary, **TB** may also be fine-tuned to fit both the current and the slope. Note that usually the lateral source/drain diffusion length **DL** is a constant for all channel lengths in a given wafer. To ensure consistency, the calibration procedure may be applied to a range of channel lengths to define an "optimized" **DL** for the given technology based on the current as well as the slope at low and high $V_{DS}$.

At this stage of the tuning process, **TB**, **DL**, **NSB**, **NBODY**, **GAMMA**, and **KAPPA** will be known. We proceed now to strong inversion to extract the remaining parameters.

### 6.3.2 Strong-Inversion Region

In strong inversion, the model formalism for the FD/SOI MOSFET is essentially based on [Vee88b]. The boundary condition for strong inversion is defined by analyses in [Yeh95]. The model parameters which can be evaluated from this region are **UO**, **THETA**, **RS/RD**, **VSAT** and **JRO**. If an LDS/LDD is present, the **LLDS/LLDD** and **NLDS** can also be evaluated here. For all structures we will assume that **RS** and **RD** are equal (and so are **LLDS** and **LLDD**) due to symmetry.

#### 6.3.2.1 Calibration Based on Linear-Region Characteristics

At low $V_{DS}$, the $I_{DS}$-$V_{GfS}$ (linear region) characteristics of the MOSFET is similar to that of a resistor with its total ON resistance $R_{ON}$ given approximately by

$$R_{ON} \equiv \frac{V_{DS}}{I_{DS}} \cong \frac{2\mathbf{RS}}{W} + \frac{L_{eff}}{WC_{of}(V_{GfS} - V_{Tf})\mu(\mathbf{UO}, \mathbf{THETA})} \quad . \quad (6.1)$$

As can be seen from (6.1), $R_{ON}$ is dependent on **UO**, **THETA**, and **RS**. To isolate the effects of **RS** and **UO/THETA**, we can show from (6.1) that $g_m/I_{DS}^2$ is nearly independent of **RS**. This allows us to first evaluate **UO** and **THETA** to fit the $g_m/I_{DS}^2$ characteristics, independent of **RS**. Once these two parameters are tuned, we can go back to (6.1) to explicitly calibrate **RS**. If an LDS/LDD is present in the structure, we first set **LLDS** to be equal to the spacer width as defined by technology, and **NLDS** to be roughly correspond to the LDD dose. Typically the LDD doping is in the mid-$10^{18}$ cm$^{-3}$ regime. When an LDS/LDD is present the resistance **RS** in (6.1) would include implicitly the ohmic component of the series resistance $R_{LDS}$ (= **LLDS/**

(q.W.**NLDS**.μ(**NLDS**).**TB**)), where μ(**NLDS**) is the mobility of the majority carriers in the LDS/LDD. However, the **RS** in the model card is the source/drain parasitic resistance *without* $R_{LDS}$. Hence, $R_{LDS}$ must be subtracted off from the evaluated (total) **RS**. Note that if, as in some technologies, the LDS/LDD is more of a source drain extension, then the effect of the LDS/LDD is to simply increase the total resistance **RS**. The non-ohmic drops in the LDD will not be important. For such cases, we recommend that the LDS/LDD feature be turned off in the model to speed up run time, as well as to improve convergence. The extraction technique for **RS** described above should then be carried out as though there were no LDS/LDD.

#### 6.3.2.2 Calibration Based on Output Characteristics at High Drain Bias

At high $V_{DS}$, and relatively large $V_{GfS}$, the current saturates in short-channel MOSFETs due to carrier velocity saturation. From model formalism we can extract the current in strong inversion at high $V_{DS}$ to be

$$I_{DS(sat)} \cong \frac{W\mu_{eff}}{2C_{of}(1+\alpha)L_{eff}} \frac{\left(Q_{cf}^2(0) - \left(\frac{I_{DS(sat)}}{W\mathbf{VSAT}}\right)^2\right)}{\left(1 + \frac{\mu_{eff}}{2\mathbf{VSAT}L_{eff}} V_{DS(sat)}\right)} \quad . \tag{6.2}$$

From (6.2) and the output $I_{DS}$-$V_{DS}$ characteristics **VSAT** can be evaluated at $V_{DS}$ close to $V_{DS(sat)}$ the saturation drain voltage at moderately high $V_{GfS}$. (The initial guess for **VSAT** can be set to $6 \times 10^6$ cm/s for NMOS.) If **VSAT** is evaluated from saturation current at very high $V_{GfS}$ (or $V_{DS}$), the power dissipation in the device may be high enough to cause self-heating [Su94]. Self-heating is not accounted for in the model and hence must be avoided in the parameter-evaluation process. Normally, for moderately high $V_{GfS}$ and at $V_{DS}$ near $V_{DS(sat)}$ self-heating is not significant. Also, at high $V_{DS}$, the parameter **FVBJT** may be used to empirically tune breakdown in strong inversion for both NMOS and PMOS. Note that **JRO** may be also roughly tuned from breakdown.

For certain applications, the transient bipolar effect in the FD/SOI MOSFET can be important, and associated parameters must be evaluated more accurately. These parameters, **JRO** and **LDIFF**, can be evaluated from transient leakage-current measurements, following the procedure described later for the PD/SOI MOSFET in Sec. 6.4.5. In the next section we will apply the above methodology to calibrate actual FD/SOI technologies only from DC characteristics.

### 6.3.3 Application to Actual FD/SOI Technologies: Example 1

The first example we will consider is an FD/SOI technology from Lincoln labs [J. Burns, Private Communication] intended for predominantly low-power applications. The information available from the process is shown in Table 6.3. We first exemplify the application of the parameter-evaluation methodology to the PMOS devices in this technology. From the process information in Table 6.3 we can define some of the (PMOS) model parameters in SOISPICE directly as indicated in Table 6.4. The next step is to determine if **NSB** is important or not. The subthreshold $I_{DS}$-$V_{GfS}$ characteristics of the PMOS devices at low-$V_{DS}$ are shown in Fig. 6.1. As pointed out earlier, the slope here is non-ideal (≈ 68 mV/dec) at relatively long channel lengths, and further, it is fairly constant when L is scaled. This indicates that fringing is not important even for the smallest device in this technology, while **NSB** is. By tuning **NSB** to get the correct swing $S_o$, we obtained a value

Table 6.3: PROCESS INFORMATION FROM LINCOLN LABS FD/SOI TECHNOLOGY

| Process details | n-channel | p-channel |
|---|---|---|
| Wafer | 50 nm Si on 380 nm BOX | Same as n-channel |
| Isolation | Etched-mesa | Same as n-channel |
| Total channel doping | $1.2 \times 10^{12}/cm^2$ Boron (calculated) | $1.45 \times 10^{12}/cm^2$ Phosphorous (calculated) |
| Poly type | n+ | p+ |
| Width | 7 μm | 7 μm |
| LDD | None | $5 \times 10^{14}/cm^2$ Boron |
| LDD length | Not applicable | 0.15 μm |
| delta-L | 0.03 μm (extracted) | 0.12 μm (extracted) |

Table 6.4: INITIAL SET OF SOISPICE MODEL PARAMETERS FOR AN FD/SOI P-CHANNEL MOSFET DEFINED FROM TECHNOLOGY

| Parameter | Value | Comment |
|---|---|---|
| TPG | +1 | p+ poly gate |
| TPS | +1 | p substrate |
| TB | 50 nm | Known from technology |
| NBODY | $2.8 \times 10^{17}$ $cm^{-3}$ | Estimated roughly as dose/TB |
| TOXF | 8 nm | Known from technology |
| TOXB | 380 nm | Known from technology |
| LLDS/LLDD | 0.15 μm | Defined from spacer width |
| DL | 0.12 μm | From Table 6.3 |
| GAMMA | 0.3 | For TOXB = 380 nm, from table 6.2 |
| KAPPA | 0.5 | For TOXB = 380 nm, from table 6.2 |

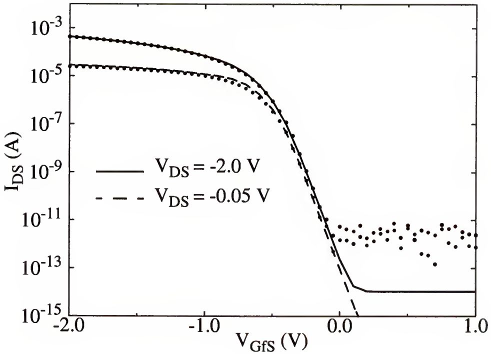


Fig. 6.4 Measured (circles) and SOISPICE-predicted (curves) subthreshold characteristics of a 0.5 μm PMOS FD/SOI technology.

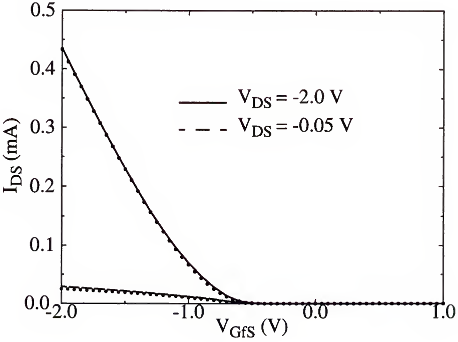


Fig. 6.5 Measured (circles) and SOISPICE-predicted (curves) linear- and saturation-region characteristics of a 0.5 μm PMOS FD/SOI technology.

of $2x10^{11}$ $cm^{-2}/eV$ (which is a fairly typical number) [Yeh95]. Once **NSB** was tuned to fit the slope, **NBODY** was then adjusted to obtain the current in the subthreshold region (at low $V_{DS}$). The new value for **NBODY** turned out to be $2.65x10^{17}$ $cm^{-3}$, which was not too different from the initial guess (in Table. 6.4) of $2.8x10^{17}$ $cm^{-3}$. Figure 6.4. shows the fit between SOISPICE-predicted and measured subthreshold region characteristics (at low and high $V_{DS}$) for a 0.5 μm PMOS device in this technology. Note that the calibrated model in Fig. 6.4 predicts the slope as well as the current at low and high $V_{DS}$ well.

The next step is to tune **UO, RS, THETA**, and **VSAT**. The first guess for **UO** was roughly estimated to be the (bulk) mobility corresponding to the given doping (**NBODY**) as extracted from standard mobility-doping curves at room temperature [Sze81]. With this initial guess, **UO**, **RS**, and **THETA**, were extracted by the procedure outlined in section 5.3.2.1. Typically, in PMOS devices **UO** is small and **THETA** is large, and this was true for this technology too. Since, the output $I_{DS}$-$V_{DS}$ characteristics were not available for this device, **VSAT** had to be tuned from the $I_{DS}$-$V_{Gfs}$ characteristics at high $V_{DS}$. Note that even though the PMOS devices had an LDD implant (see Table 6.3), the dose was high enough to render the LDD a source/drain extension. Hence, **RS** here accounts for the source/drain parasitic resistance and any other resistance due to the source/drain extension.

Figure 6.5 shows the model-calibrated $I_{DS}$-$V_{Gfs}$ characteristics fit to the measured data in the linear and saturation regions. Table 6.5 shows the list of evaluated model parameters along with their values for this technology. The model parameters in Table 6.5

were also used to predict the characteristics of a 0.25 μm PMOS device in this technology as shown in Fig. 6.6. All the model parameters were the same, except that **DL** had to be decreased from 0.12 μm to 0.01 μm. It is possible that the extracted value of **DL** (given in Table 6.3) was not accurate in this technology. This fact was not evident in the longer channel device, as any error in **DL** will affect the characteristics of a shorter-channel device much more than those of a longer-channel device. Also note that for the given bias conditions (up to 2V drain bias) these characteristics did not show effects due to high-fields such as impact ionization or the parasitic BJT. Therefore, the model was not calibrated to properly account for these high-field effects.

The above methodology was also applied to NMOS devices in this technology. The model-calibrated characteristics agree well with the measured data in the linear and saturation regions for the 0.5 μm devices as shown in Fig. 6.7, but in the subthreshold region the measured data exhibits significant edge conduction as indicated in Fig. 6.8 which is not accounted for in the model. An interesting observation is that for the shorter device (L = 0.25 μm), **NBODY** had to be increased, indicating the possibility of reverse short-channel effect in the NMOS devices. This highlights the utility of the calibration process when applied to a physical model, wherein insight into technology can be attained.

### 6.3.4 Application to Actual FD/SOI Technologies: Example 2

We will consider another technology to further demonstrate the utility of the systematic evaluation process. The FD/SOI technology that we consider here is a generic one from MIT [L. Su, Private Communication]. In the previous example, the effects due to fringing were insignificant. Hence, **GAMMA** and **KAPPA** did not affect the subthreshold

Table 6.5: EVALUATED PARAMETERS FOR PMOS DEVICES CORRESPONDING TO THE LINCOLN LABS TECHNOLOGY

| Parameter | Value | Comment |
|---|---|---|
| NSB | $2\text{x}10^{11}$ cm$^{-2}$/eV | Surface state density important |
| NBODY | $2.65\text{x}10^{17}$ cm$^{-3}$ | Tuned from subthreshold current |
| UO | 125 cm$^2$/(V.s) | Typical (low) value for PMOS |
| THETA | $2.5\text{x}10^{-6}$ cm/V | Typical (high) value for PMOS |
| RS/RD | 415 ohm-μm | Large RS/RD due to thin SOI film |
| VSAT | $8\text{x}10^6$ cm/s | Larger than typical values for PMOS |

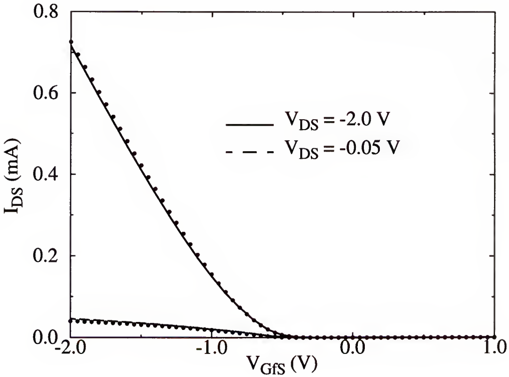


Fig. 6.6 Measured (circles) and SOISPICE-predicted (curves) linear- and saturation-region characteristics of a 0.25 μm PMOS FD/SOI technology.

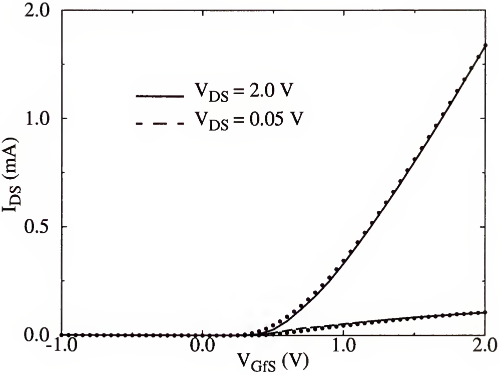


Fig. 6.7 Measured (circles) and SOISPICE-predicted (curves) linear- and saturation-region characteristics of a 0.5 μm NMOS FD/SOI technology.

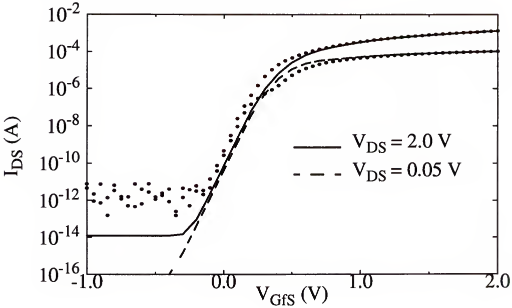


Fig. 6.8 Measured (circles) and SOISPICE-predicted (curves) subthreshold characteristics of a 0.5 μm NMOS FD/SOI technology showing edge conduction.

Table 6.6: INITIAL MODEL PARAMETER SET DEFINED FROM PROCESS INFORMATION FOR AN MIT FD/SOI TECHNOLOGY

| Parameter | Value | Comment |
|---|---|---|
| TOXF | 9 nm | Defined from technology |
| TB | 42 nm | Defined from technology |
| TOXB | 360 nm | Defined from technology |
| W | 10 μm | Defined from technology |
| NGATE/NDS | $5 \times 10^{19}$ cm$^{-3}$ | Defined from technology |
| TPG | +1 | n+ poly gate |
| TPS | -1 | p substrate |
| RS/RD | 400 ohm-μm | Extracted from measurements |
| NBODY | $5 \times 10^{16}$ cm$^{-3}$ | Estimated from dose |

characteristics much. Also, the output $I_{DS}$-$V_{DS}$ characteristics were not available to completely calibrate all model parameters (e.g., **JRO** that controls the gain of the parasitic bipolar near breakdown at high $V_{DS}$). In this example, the devices exhibit fringing effects in the subthreshold characteristics, and further the output characteristics are available to calibrate parameters like **JRO**.

The initial model parameters constructed from available process information are listed in Table 6.6. All devices are NMOS. The (effective) channel lengths ranged from 0.55 μm to 0.23 μm. From the subthreshold $I_{DS}$-$V_{Gfs}$ characteristics for a long channel device ($L_{eff}$ = 0.55 μm), we once again find here that the slope is non-ideal (≈ 70 mV/dec) indicating the presence of surface states. A value of $1.2\text{x}10^{11}$ $cm^{-2}$/eV was extracted for **NSB** based on $S_o$. As L is scaled, $S_o$ increases indicating that fringing is important in this technology. The initial values for **GAMMA** and **KAPPA** were first defined directly from Table 6.2. to be 0.3 and 0.5, respectively. While the above value for **GAMMA** was adequate to fit $S_o$, **KAPPA** had to be increased to 0.8 to fit the slope at high $V_{DS}$. It is possible that this increase in **KAPPA** partly reflects punch-through at low gate bias in the actual measured characteristics, which is not accounted for in the model. Neither the value of **TB** nor **NBODY** had to be changed. In all the simulations **DL** was set to zero as information on the effective channel length was directly available (from standard shift-to-ratio extraction techniques). Figure 6.9 shows the measured and simulated subthreshold characteristics at low $V_{DS}$ for different L. Note how $S_o$ increases for increasing L due to fringing, and also how the model predicts this increase well. Figure 6.10 shows the measured and simulated subthreshold characteristics at low and high $V_{DS}$ for a 0.3 μm device in this technology. (Note increase in S at high $V_{DS}$, due to increased fringing is modeled well.)

Now, from the linear region characteristics, **UO** and **THETA** were tuned to be 550 $cm^2/(V.s)$ and $1.9 \times 10^{-6}$ cm/V. The parasitic resistance **RS** was set to its extracted value of 400 ohm-μm as indicated in Table. 6.6. Figure 6.11 shows the model-predicted and measured linear- and saturation-region characteristics for this 0.3 μm device. From the output characteristics near saturation (but at low power levels), **VSAT** was evaluated to be $8 \times 10^6$ cm/s, which is a typical value for NMOS devices. Also, by (roughly) tuning to get the right breakdown voltage, **JRO** was estimated to be $1 \times 10^{-16}$ A/m, which is a typical value for recombination in the heavily doped, quasi-neutral source [Fos81]. The impact ionization coefficients **ALPHA** and **BETA** were set to their default (physical) values of $2.45 \times 10^6$ /cm and $1.92 \times 10^6$ V/cm, respectively. The resulting model-calibrated output characteristics agree well with the measured data, including near the breakdown region. Note that in high-power regions the model over-predicts the drive current compared to the measured data which exhibits self-heating. The model does not account for self-heating as mentioned earlier.

Note that the model calibration here has been done based only on DC I-V characteristics. Some of the parameters which are important in transients can be estimated from technology, for e.g., the gate-source overlap capacitance **CGFSO** is approximately **DL**$*\varepsilon_{ox}/$**TOXF**. They can also be directly tuned from transient measurements, if necessary. Having demonstrated the use of the parameter-evaluation methodology for FD/SOI MOSFETs in SOISPICE, we now turn our attention to PD/SOI MOSFETs, where peculiar floating-body effects [Suh95] have to be properly accounted for in the calibration process.

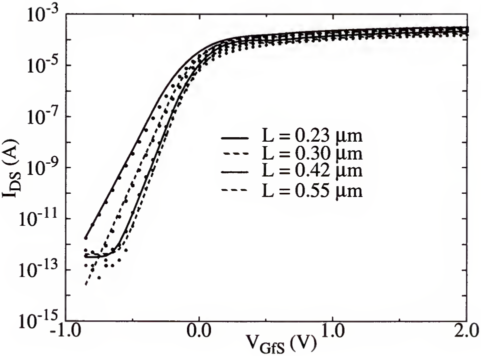


Fig. 6.9 Measured (points) and simulated (curves) $I_{DS}$-$V_{GfS}$ characteristics in the sub-threshold region at low $V_{DS}$ for varying L.

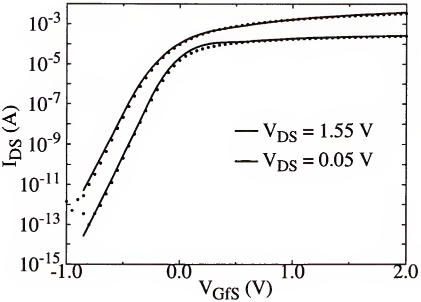


Fig. 6.10 Measured (points) and simulated (curves) $I_{DS}$-$V_{GfS}$ characteristics in the sub-threshold region of a 0.3 µm FD/SOI MOSFET.

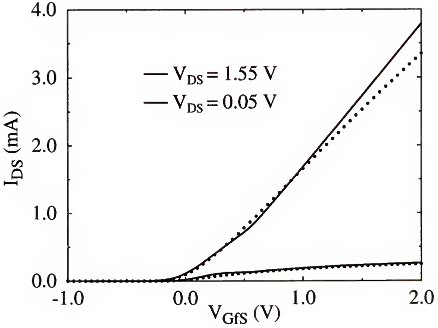


Fig. 6.11 Measured (points) and simulated (curves) $I_{DS}$-$V_{GfS}$ characteristics of a 0.3 µm FD/SOI MOSFET in the linear and saturation regions.

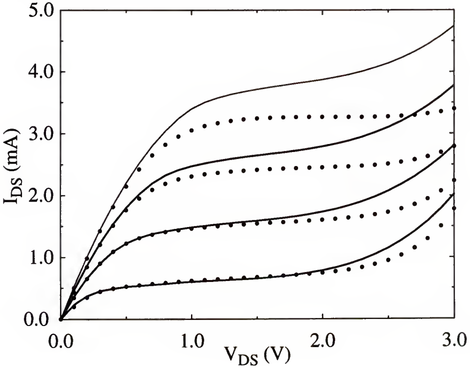


Fig. 6.12 Measured (points) and simulated (curves) output $I_{DS}$-$V_{DS}$ characteristics of a 0.3 µm FD/SOI MOSFET for varying $V_{GfS}$.

## 6.4 Parameter Evaluation for PD/SOI MOSFETs

The PD/SOI MOSFET is distinctly different from the FD/SOI MOSFET due to the presence of a neutral body [Suh95]. The neutral body gives rise to peculiar DC and transient floating-body effects such as kinks in the I-V characteristics and dynamic variation of threshold voltage [Suh94b]. Consequently, a new model for the PD/SOI MOSFET in SOISPICE, which is based on the thin-film accumulated (TFA) approximation [Lim84], was recently developed by Suh [Suh95]. A non-local model for impact ionization developed in Chapter 2 was also incorporated to properly account for kinks and breakdown voltage. The predictive capability of the PD/SOI model has been widely demonstrated [Suh94b, Suh95]. Here we show how a systematic parameter-evaluation methodology for the PD/SOI MOSFET, similar in approach to that for the FD/SOI MOSFET but inherently different due to the presence of a neutral body, can be used to evaluate model parameters for a given technology.

The model parameters for the PD/SOI MOSFET in SOISPICE are listed in Table 6.7. As for the FD/SOI MOSFET, some of these parameters can be defined directly based on technology, while others have to evaluated based on measured data. The *critical* parameters for the PD/SOI MOSFET that usually have to be evaluated (from measured data in DC) are **TB, NBL, NBH, JRO, M, DL, TAUO, UO, RS/RD, THETA**, and **VSAT**. If the application demands calibration of the transient bipolar effect described in the previous chapter, then two additional model parameters, **SEFF** and **LDIFF**, have to be evaluated based on either high-speed transient measurements [Pel95], or possibly from C-V measurements. We first outline the methodology for parameter evaluation from measured DC

Table 6.7: PD/SOI MODEL PARAMETERS IN SOISPICE

| Name | Description | Typical range of values |
|---|---|---|
| VFBF | Front-gate flatband voltage | Calculated if defaulted |
| VFBB | Back-gate flatband voltage | Calculated if defaulted |
| WKF | Front-gate work function difference | Calculated if defaulted |
| WKB | Back-gate work function difference | Calculated if defaulted |
| NQFF | Front oxide fixed charge | ~ $10^{10}$ $cm^{-2}$ |
| NQFB | Back oxide fixed charge | ~$10^{10}$-$10^{11}$ $cm^{-2}$ |
| TOXF | Front-gate oxide thickness | 4-10 nm |
| TOXB | Back-gate oxide thickness | 80-400 nm |
| NSUB | Substrate doping density | $10^{15}$-$10^{17}$ $cm^{-3}$ |
| NGATE | Poly gate doping density | ~ $10^{20}$ $cm^{-3}$ |
| TPG | Type of gate material:<br>+1) opposite to body<br>-1) same as body<br>0) Aluminum | +1 |
| TPS | Type of substrate material:<br>+1) opposite to body<br>-1) same as body | -1 |
| TF | Total silicon film thickness | 100-200 nm |
| TB | Effective film thickness | 30-50 nm |
| THALO | Halo thickness | 50-100 nm |
| NBL | Low body doping density | > $10^{17}$ $cm^{-3}$ |
| NBH | High body doping density | ~ $10^{18}$ $cm^{-3}$ |
| NHALO | Halo doping density | ~ $10^{18}$ $cm^{-3}$ |

Table 6.7: -- (Continued)

| Name | Description | Typical range of values |
|---|---|---|
| UO | Zero-field mobility | 200-600 $cm^2/(V.s)$ (NMOS)<br>70-400 $cm^2/(V.s)$ (PMOS) |
| THETA | Mobility degradation coefficient | $(0.1\text{-}3)x10^{-6}$ cm/V |
| BFACT | $V_{DS}$-averaging factor for mobility degradation | 0.1-0.5 |
| VSAT | Carrier saturated drift velocity | $(0.5\text{-}1)x10^{7}$ cm/s |
| ZETA | On/off flag for charge sharing (0 for no charge sharing) | 1 |
| ALPHA | Impact-ionization parameter $\alpha_0$ | $2.45x10^{6}$ /cm |
| BETA | Impact-ionization parameter $\beta_0$ | $1.92x10^{6}$ V/cm |
| TAUO | Carrier life time in the body | $10^{-5}\text{-}10^{-8}$ s |
| LDS | LDS region length (0 for no LDS) | 0.05-0.2 μm |
| LDD | LDD region length (0 for no LDD) | 0.05-0.2 μm |
| NLDS | LDD/LDS doping density | ~ $10^{18}$ $cm^{-3}$ |
| NDS | Source/drain doping density | > $5x10^{19}$ $cm^{-3}$ |
| JRO | Body-source junction recombination current coefficient | $10^{-11}\text{-}10^{-9}$ A./m |
| M | Junction non-ideality factor | 1.5-2.0 |
| SEFF | Effective surface recombination velocity in the source | $5x10^{4}\text{-}10^{5}$ cm/s |
| ETA | On/off flag for DICE (0 for no DICE) | 1 |
| LMOD | On/off flag for channel-length modulation | 1 |
| CGFDO | Gate-drain overlap capacitance | ~ $10^{-10}$ F/m |
| CGFSO | Gate-source overlap capacitance | ~ $10^{-10}$ F/m |

Table 6.7: -- (Continued)

| Name | Description | Typical range of values |
|---|---|---|
| CGFBO | Gate-body overlap capacitance | ~ $10^{-10}$ F/m |
| RHOSD | Source/drain sheet resistance | Ohms/sq |
| RHOB | Body sheet resistance | Ohms/sq |
| RD | Specific drain parasitic resistance | 200-500 $\Omega$-$\mu$m |
| RS | Specific source parasitic resistance | 200-500 $\Omega$-$\mu$m |
| RB | Body parasitic resistance | > $10^5$ $\Omega$ |
| DL | Channel-length reduction | 0.05-0.2 $\mu$m |
| DW | Channel-width reduction | 0.1-0.5 $\mu$m |
| LDIFF | Effective diffusion length in S/D | 0.1-0.5 $\mu$m |

data in various regions of operation, and subsequently exemplify its use by applying it to actual technologies. Then, we will consider extension of the methodology for application in transients, e.g., calibration of the transient bipolar effect.

### 6.4.1 Subthreshold Region

In the subthreshold region, the current conduction mechanism in a PD/SOI MOSFET is predominantly by carrier diffusion, similar to that in a FD/SOI MOSFET. However, there are no effects due to fringing here, unlike the FD/SOI MOSFET, due to the presence of the neutral layer [Suh95]. The slope and the current in the subthreshold region can be used to calibrate some of the key parameters such as **TB**, **NBL**, **DL**, **JRO**, and **M**.

#### 6.4.1.1 Calibration Based on Slope/Current at Low Drain Bias

We first consider the measured subthreshold $I_{DS}$-$V_{Gfs}$ characteristics at low drain bias ($V_{DS}$ 100 mV). The subthreshold slope $S_o$ here is given approximately by $60(1+\alpha)$ where $\alpha = C_b/C_{of}$, with $C_b$ ($= \varepsilon_s/$**TB**) and $C_{of}$ ($= \varepsilon_{ox}/$**TOXF**) being the body-depletion and front-oxide capacitances, respectively. Hence, from the slope (with knowledge of **TOXF** from technology), a value for **TB** can be estimated fairly accurately. Note that $S_o$ is nearly independent of the effective channel length $L_{eff}$ as shown in Fig. 6.13.

The doping densities **NBL** (and **NBH**) effectively model any retrograde doping in the channel [Suh95]. However, only **NBL** has an effect on the threshold voltage. Hence, **NBL** can be tuned based on the subthreshold current at low $V_{DS}$. A correlation between **TB** and **NBL** is worth pointing out: the maximum depletion width [Sze81], $x_{d(max)}$(**NBL**), must be greater than **TB** for the model to be strictly valid. (**DL** can also be tuned in this region.)

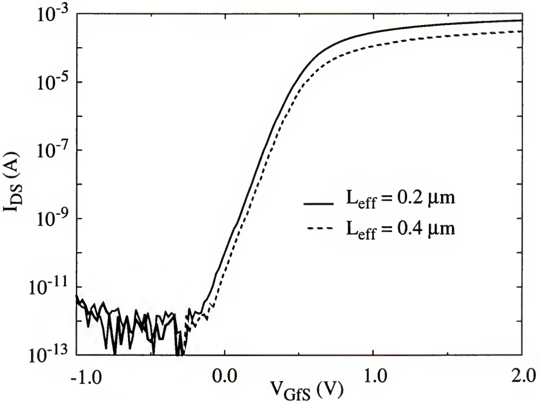


Fig. 6.13 Measured $I_{DS}$-$V_{GfS}$ characteristics of PD/SOI MOSFETs for varying $L_{eff}$. Note that the slope $S_o$ is nearly independent of $L_{eff}$.

### 6.4.1.2 Calibration Based on Slope/Current at High Drain Bias

Next we consider subthreshold $I_{DS}$-$V_{GfS}$ characteristics at higher $V_{DS}$, but *before* the onset of the parasitic BJT or drain-source breakdown. In this region, impact ionization drives the body, thereby lowering the threshold voltage. This gives rise to a kink in the subthreshold region at high $V_{DS}$ [Suh95], wherein the current increases rapidly even for a small increase in gate bias. The slope and the magnitude of this kink is controlled by the equivalence between the generation due to impact ionization and recombination. The non-ideal component of recombination during this kink (in the body-source space-charge region as opposed to the quasi-neutral regions), gives rise to the supra-ideal slope, i.e., $S <$ 60 mV/dec. From model formalism [Suh95], we can derive S (after the occurrence of the kink) to be:

$$S \cong S_0 - 60\mathbf{M}\alpha \qquad . \qquad (6.3)$$

Now, **M** can be estimated from the subthreshold slope S after the kink. As is characteristic of non-ideal recombination, **M** is greater than 1, and typically lies between 1.5 and 2. The magnitude of the shift in current (due to threshold voltage lowering), which is governed by the recombination current coefficient, can be used to obtain **JRO**. Note that **ALPHA** and **BETA** (impact ionization coefficients) for electrons (in NMOS) can be assumed to have their default (physical) values. For holes (in PMOS), **ALPHA** and **BETA** are usually not important, as the impact-ionization rate for holes is much smaller than that for electrons. If impact ionization is important in the given PMOS technology, then **ALPHA** and **BETA** have to be tuned from the current, in addition to **JRO**.

At this stage of the tuning process, **TB**, **NBL**, **DL**, **JRO**, and **M** will be known. We proceed now to strong inversion to extract the remaining parameters.

### 6.4.2 Strong-Inversion Region

The model parameters which can be evaluated from the strong-inversion region are **UO**, **THETA**, **RS/RD**, **TAUO**, and **VSAT** (and also if **LLDD/LLDS**, if present).

#### 6.4.2.1 Calibration Based on Linear-Region Characteristics

In strong-inversion ($V_{GfS} > V_{TS}$), $I_{DS}$-$V_{GfS}$ characteristics at constant and very low $V_{DS}$ (< 100 mV) yield information on **UO**, **THETA**, and **RS/RD**. The procedure for extracting these parameters is analogous to that for the FD/SOI MOSFET (outlined in Section 6.3.2.1).

#### 6.4.2.2 Calibration Based on Output Characteristics at High Drain Bias

**TAUO**, which is an important parameter that drives some of the floating-body effects, can be estimated from $I_{DS}$-$V_{DS}$ characteristics at $V_{DS}$ near $V_{DS(sat)}$ and relatively low $V_{GfS}$ such that the current saturation is controlled by pinch-off ($V_{GfS} \sim V_{TS}$). The latter condition will ensure that only **TAUO**, and not any other parameter such as **VSAT**, controls $I_{DS(sat)}$ for these bias conditions. The increase in the saturation current (over that of a tied-body device) for this bias condition is due to the thermal generation governed by **TAUO**. Note that, if a test device with a body contact is available for this technology, then **TAUO** can be better estimated by measuring $I_{DS}$-$V_{DS}$ characteristics of tied- and floating-body devices.

An important point to note is that **JRO** evaluated from the subthreshold region should predict the current kink in the strong-inversion region too, as the same mechanism is responsible for both subthreshold- and saturation-region current kinks. The saturation velocity **VSAT** can now be estimated by examining high-$V_{Gfs}$ $I_{DS}$-$V_{DS}$ characteristics (at $V_{DS}$ near $V_{DS(sat)}$) from a procedure similar to that described for the FD/SOI MOSFET in Section 6.3.2.2. Finally, the two parameters (**SEFF** and **LDIFF**) associated with the new parasitic bipolar modeling in Chapter 5 should be extracted from transient leakage-current measurements, to be discussed later, or from capacitance-voltage measurements.

We will now exemplify the utility of the evaluation process in DC by applying it to two PD/SOI technologies. Further, we will also indicate how this process can be extended to calibrate the bipolar effect, and therefore the BiMOS model developed in Chapter 5, from transient measurements.

### 6.4.3 Application to Actual PD/SOI Technologies: Example 1

The first example we will consider is a technology from Texas Instruments [Ted Houston, Private Communication]. Information available from the process was used to construct the initial model parameter set (for NMOS devices) shown in Table. 6.8.

We begin the evaluation process by focusing on the subthreshold characteristics. The measured $S_0$, which is about 90 mV/dec, yielded a value of 41 nm for **TB**. Next, from the supra-ideal slope ($\approx$ 36 mV/dec) at high $V_{DS}$, which is common in PD/SOI MOSFETs, a value of 2 for **M** was obtained. Also from the current at high $V_{DS}$ in the subthreshold region, **JRO** was tuned to be $1\text{x}10^{-11}$ A/m. This value is typical for recombination current coefficients in the space-charge region. Fig. 6.14 shows that the model tuned to the measured data in the subthreshold region at low and high $V_{DS}$. Note that both the slope as well as the current are predicted well. Next we turn to strong-inversion region at low $V_{DS}$, where **UO**, **THETA**, and **RS/RD** are evaluated “iteratively” by the process described for

Table 6.8: INITIAL MODEL PARAMETER SET DEFINED FROM PROCESS INFORMATION FOR A TI PD/SOI TECHNOLOGY

| Parameter | Value | Comment |
|---|---|---|
| TOXF | 7 nm | Defined from technology |
| TF | 120 nm | Defined from technology |
| TOXB | 400 nm | Defined from technology |
| W | 5 μm | Defined from technology |
| NGATE/NDS | $5x10^{19}$ $cm^{-3}$ | Defined from technology |
| TPG | +1 | n+ poly gate |
| TPS | -1 | p substrate |
| $L_{eff}$ | 0.2 μm | Defined from technology and also from extraction of DL |

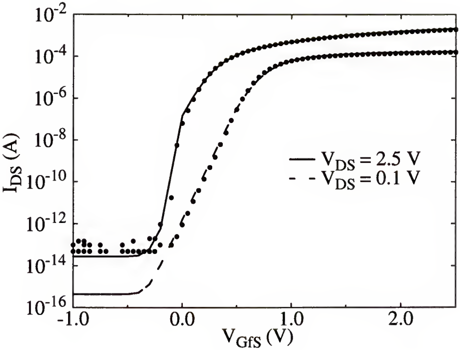


Fig. 6.14 Measured (points) and model-calibrated (curves) subthreshold characteristics of a 0.2 μm TI PD/SOI MOSFET at low and high $V_{DS}$.

for the FD/SOI MOSFET. The next parameter evaluated is **TAUO** from low-$V_{GfS}$ (but still in strong inversion) $I_{DS}$-$V_{DS}$ characteristics near saturation (before the kink), where the dominant generation current is due to thermal generation. A value of $10^{-7}$ s is obtained for this technology. Finally, **VSAT** was tuned from relatively high $V_{GfS}$ $I_{DS}$-$V_{DS}$ characteristics to be $10^{7}$ cm/s. The measured and simulated $I_{DS}$-$V_{GfS}$ in Fig. 6.15, as well as the output characteristics shown in Fig. 6.16 are in good agreement now. This completes the evaluation process for this technology based on DC I-V characteristics. The evaluated parameters for the NMOS devices are listed in Table. 6.9.

### 6.4.4 Application to Actual PD/SOI Technologies: Example 2

The second example we consider is a technology from IBM [Jack Sun, Private Communication]. Once again, based on the given process information, the initial model set in Table. 6.10 was developed. The procedure for evaluating parameters for this technology is similar to that described for the TI technology. An additional parameter that was tuned here was **NBH** to obtain the correct breakdown voltage. The results of the tuning show good agreement between model-calibrated characteristics and measured data in both the subthreshold and the strong-inversion regions of operation as indicated by Figs 6.17-6.19 for an $L_{eff} = 0.2$ μm NMOS device in this technology. The model also tracks the measurements well, including in the breakdown region, when the channel length is varied, as shown in Fig. 6.20. The single set of parameters evaluated for this technology are given in Table. 6.11. (Note that the gate-induced drain leakage (GIDL) current is significant at very low (negative) $V_{GfS}$ and high $V_{DS}$, and that none of the model parameters were evaluated in this region, since the current version of SOISPICE does not model GIDL.)

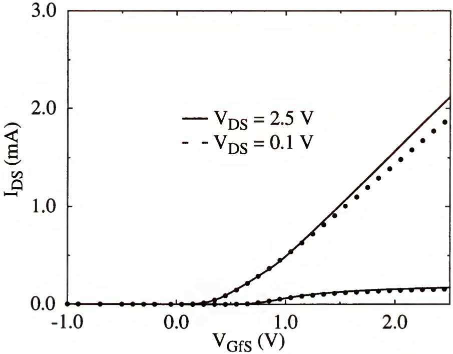


Fig. 6.15 Measured (points) and model-calibrated (curves) linear (low $V_{DS}$) and saturation (high $V_{DS}$) region characteristics of a 0.2 μm TI PD/SOI MOSFET.

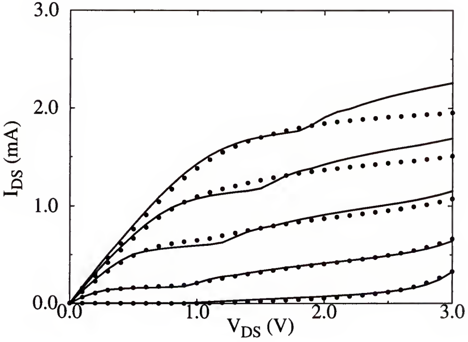


Fig. 6.16 Measured (points) and simulated (curves) output $I_{DS}$-$V_{DS}$ characteristics of a 0.2 μm TI PD/SOI MOSFET for $V_{GfS}$ varying from 0.5-2.5 V.

Table 6.9: MODEL PARAMETERS EVALUATED FOR A TI PD/SOI TECHNOLOGY

| Parameter | Value |
|---|---|
| TB | 42 nm |
| NBL | $4.5 \times 10^{17}$ cm$^{-3}$ |
| M | 2 |
| JRO | $1 \times 10^{-11}$ A/m |
| UO | 450 cm$^2$/(V.s) |
| THETA | $1.2 \times 10^{-6}$ cm/V |
| RS/RD | 1000 ohm-µm |
| TAUO | $10^{-7}$ s |
| VSAT | $10^7$ cm/s |

Table 6.10: INITIAL MODEL PARAMETER SET DEFINED FROM PROCESS INFORMATION FOR AN IBM PD/SOI TECHNOLOGY

| Parameter | Value | Comment |
|---|---|---|
| TOXF | 5 nm | Defined from technology |
| TF | 75 nm | Defined from technology |
| TOXB | 400 nm | Defined from technology |
| W | 10 µm | Defined from technology |
| NGATE/NDS | $5 \times 10^{19}$ cm$^{-3}$ | Defined from technology |
| TPG | +1 | n+ poly gate |
| TPS | -1 | p substrate |
| $L_{eff}$ | 0.3 µm | Defined from technology and also from extraction of DL |

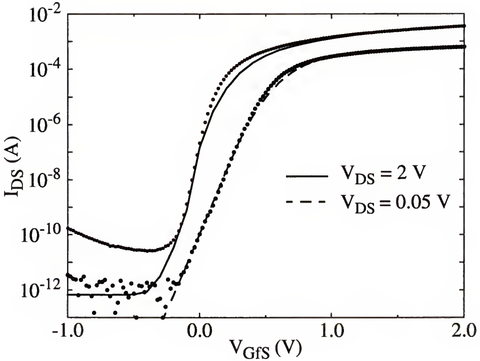


Fig. 6.17 Measured (points) and model-calibrated (curves) subthreshold characteristics of a 0.2 μm IBM PD/SOI MOSFET at low and high $V_{DS}$.

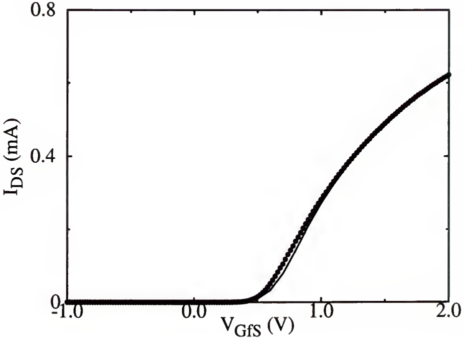


Fig. 6.18 Measured (points) and model-calibrated (curves) linear region ($V_{DS} = 0.05$ V) characteristics of a 0.2 μm IBM PD/SOI MOSFET.

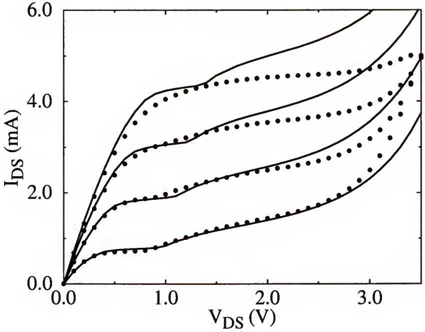


Fig. 6.19 Measured (points) and simulated (curves) output $I_{DS}$-$V_{DS}$ characteristics of a 0.2 μm IBM PD/SOI MOSFET for $V_{Gfs}$ varying from 0.5-2.5 V.

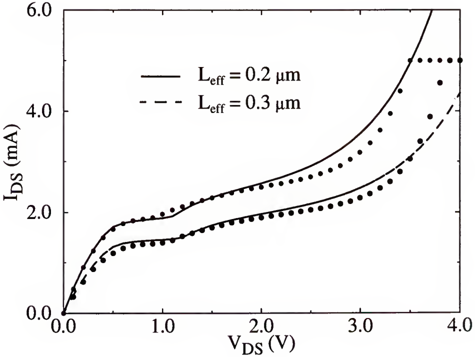


Fig. 6.20 Measured (points) and simulated (curves) output $I_{DS}$-$V_{DS}$ characteristics of a IBM PD/SOI MOSFETs for varying $L_{eff}$.

Table 6.11: MODEL PARAMETERS EVALUATED FOR AN IBM PD/SOI TECHNOLOGY

| Parameter | Value |
|---|---|
| TB | 35 nm |
| NBL | 3.8x$10^{17}$ cm-$^{3}$ |
| M | 2 |
| JRO | 7x$10^{-11}$ A/m |
| UO | 520 cm$^{2}$/(V.s) |
| THETA | 2.5x$10^{-6}$ cm/V |
| RS/RD | 200 ohm-μm |
| TAUO | $10^{-9}$ s |
| VSAT | 7.5x$10^{6}$ cm/s |
| NBH | $10^{18}$ cm$^{-3}$ |

Having demonstrated the utility of the parameter evaluation algorithm based on DC I-V characteristics, we now turn our attention to transients. As mentioned earlier, some of the overlap capacitances in the model can either be estimated, or tuned from inverter-chain delay measurements. In addition to these (extrinsic) model parameters, there are other intrinsic model parameters which play an important role in controlling certain transients. We will discuss in the next section how these parameters can be evaluated, given specific transient measurements.

### 6.4.5 Extension of PD/SOI Methodology to Calibrate the Transient Bipolar Effect

In order to complete the calibration of the BiMOS model, some of the intrinsic model parameters that control the bipolar effect must be evaluated. For example, the parameters **LDIFF** and **SEFF** are crucial in determining the peak (as well as the shape) of the transient bipolar current discussed in the previous chapter. The parameter **SEFF** controls the recombination current for high $V_{BS}$, while **LDIFF** defines the stored charge in the source (and hence, part of the diffusion capacitance). Since these parameters govern the behavior of the transient BJT, they can be evaluated from pass-transistor transients, such as the one described in the previous chapter, where the bipolar is activated. Usually these pulsed measurements have to be performed using a high-speed set up [Pel95]. The experiment basically involves pulsing the source rapidly (at a fall rate of $V_{DD}/t_f$), with the gate and drain held at 0 and $V_{DD}$ respectively. Now with reference to Chapter 5, if the fall rate is large such that $C_{of}V_{DD}/t_f > I_R(V_{BS})$, then the peak will be predominantly controlled by the diffusion capacitance ($\propto$ **LDIFF**). Hence, we can obtain **LDIFF** by tuning for the peak BJT current. After the fall of the pulse, the ratio of recombination to diffusion capacitance dictates how quickly the current decays. Since the diffusion capacitance would already have been evaluated from the peak current, **SEFF** can now be tuned to fit the decay of the pass-transistor current. Note that the other component of recombination (in the SCR) involving **JRO** and **M** is calibrated based on DC characteristics as described previously in this chapter.

As an example of extension of the evaluation technique in transient, we consider an IBM technology where we first evaluated most of the model parameters based on the DC I-V characteristics. Then, from pass-transistor measurements [Ass96] we tuned **LDIFF** to obtain the peak transient drain current. For these devices **SEFF** was set to its default, but typical value of $10^5$ cm/s. The peak measured value of the transient current was about 3.3 μA/μm, which is close to the model-simulated transient current shown in Fig. 6.21.

## 6.5 Summary/Conclusions

In this chapter, a systematic and efficient physics-based parameter-evaluation methodology was developed for both the FD/ and PD/SOI MOSFET models in SOISPICE. The methodology involves calibrating (physical and/or structure-dependent) model parameters, given measured DC I-V characteristics, preceded by straightforward and accurate estimations based on the characterization of the SOI technology. Since certain parameters have a characteristic signature in a given region of operation, it is possible to isolate one or more model parameters of interest. This methodology for parameter evaluation is physical, yet relatively straightforward. Further, it can also provide useful insight into technology as the resulting model parameters can be correlated

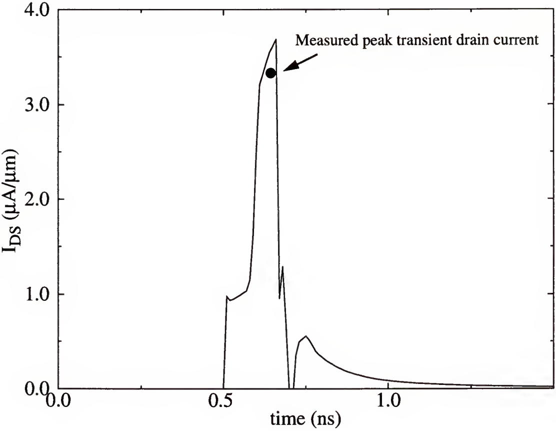


Fig. 6.21 SOISPICE predicted pass-transistor transient current through the drain for an $L_{eff} = 0.2$ μm PD/SOI MOSFET. The source was pulsed from 1.75 to 0 V at a fall rate of 1.75V/0.16ns. The measured peak drain current was 3.3 μA/μm.

to the process. The utility of the methodology was demonstrated by applying it to actual FD/ and PD/SOI technologies.

For application in automated parameter-evaluation schemes, local optimization of parameters may be done if necessary. For example, for the PD/SOI MOSFET, **TB** and **NBL** can be optimized from the subthreshold slope and current at low $V_{DS}$. Global optimization may lead to non-physical values for some of the parameters. The evaluation technique can further be extended to calibrate the transient bipolar effect, which can be important in certain applications.

# CHAPTER 7
# SUMMARY AND SUGGESTIONS FOR FUTURE WORK

## 7.1 Summary

The research described in this dissertation concerned development of compact physical models for non-local and floating-body effects for application in scaled SOI CMOS technology. The important contributions of this work are summarized below.

First, the effect of velocity saturation on the drive current of FD/SOI MOSFETs was studied. Severe limitation of current drive enhancement in deep-submicron FD/SOI MOSFETs was reported based on SOISPICE simulations supported by measurements of test devices and analytical insight. The study, however, did not include the effect of carrier velocity overshoot, which is a non-local phenomenon. Inclusion of velocity overshoot, with the aid of a new model, indicated that due to its higher low-field mobility, part of the enhancement in current drive of FD/SOI MOSFETs will be retained.

Second, a compact and physical model for non-local impact ionization in scaled SOI MOSFETs was developed for the first time. The model was then implemented as "post-processing" in SOISPICE, and extensively verified via simulations of breakdown in FD/ and PD/SOI MOSFETs, in addition to predictions of kinks in PD/SOI MOSFETs. SOISPICE simulations were used to gain insight into optimal device/circuit design. It was shown that the impact ionization-driven breakdown in DC will not be a show stopper in scaled SOI MOSFETs. The need for an LDD in scaled SOI technologies was assessed; its efficacy seems to be unwarranted in deep-submicron technologies because of the nonlocal nature of impact ionization, and, for $L < 0.15$ µm, possibly velocity overshoot.

Third, it was shown that an impact ionization-driven subthreshold kink can occur in highly scaled FD/SOI MOSFETs. The mechanism for this kink was explained, and the resulting insight was used to qualify the meaning of FD/SOI. The results here suggest that the off-state leakage current $I_{off}$ can be high in FD/SOI MOSFETs because of a kink and/or charge sharing, and hence control of it may require harder design tradeoffs than previously thought.

Fourth, a comprehensive quasi-2D BiMOS model for both the transport and the charge for the parasitic BJT was developed for both PD/ and FD/SOI MOSFETs. The model in SOISPICE was verified through copious transient MEDICI simulations where the parasitic bipolar was activated due to dynamic body charging. Insight gained from the model was used to identify a new means of controlling the transient bipolar effect, namely, enhancing the diffusion capacitance. It was shown that in scaled technologies, the diffusion capacitance can be important in addition to recombination in controlling the peak transient current. It was also indicated that the efficacy of increasing diffusion capacitance may depend on the nature of application.

Finally, a physics-based systematic parameter-evaluation methodology was outlined for the FD/ and the PD/SOI MOSFET models in SOISPICE. This calibration process, which was based on measured DC I-V characteristics as well as the SOI technology, was applied to evaluate model parameters for a wide range of actual FD/ and PD/SOI technologies. In addition, it was also used to systematically verify the models (existing and newly developed) in SOISPICE. The resulting physical model parameters, as indicated, can also shed insight into the given technology. Extension of the methodology for calibrating the PD/SOI BiMOS model was also indicated.

## 7.2 Suggestions for Future Work

First, we suggest application of the physical transient bipolar model to comprehensively study single event upsets (SEU) and soft-error rate (SER) in SOI technologies. The transient bipolar can significantly increase the probability of SEU in SOI devices. Hence, to properly study these effects at the device and circuit levels, a physical model such as the one developed in Chapter 5 has to be used. The idea of enhancing diffusion capacitance to suppress the transient bipolar, and consequently reducing SEU, should also be explored thoroughly.

Second, we recommend SOISPICE simulations with the new BiMOS model to study the significance of the parasitic bipolar in certain (critical) circuits. For example a more thorough study of the loss of stored charge in DRAM cell capacitors for a realistic technology, with typical switching sequences on the bit and word lines, could be carried out.

Third, the parameter-evaluation algorithm outlined in Chapter 5 can be refined based on C-V measurements. For example, a high-speed pulse-measurement set up may not always be available for calibrating the parasitic bipolar effect. However, small-signal measurements, which are in general simpler to make, can alternatively be used to calibrate the model. Depending on the bias condition and the frequency of the small signal, different recombination/generation and diffusion capacitance-related parameters can be isolated; hence, a physics-based approach to calibration can be reliably carried out. (Small-signal models in SOISPICE will have to be refined to ensure that the AC charge dynamics are accounted for properly.) Again, as described in Chapter 6, the calibration procedure must be performed in regions where self-heating is minimal. The evolution of the parameter-evaluation algorithm will continue to be critical for new model development in SOISPICE, and its subsequent use in reliable circuit simulation.

Lastly, the velocity overshoot model in Chapter 2 has to be verified through actual measured data. To avoid confusion between overshoot from any other short-channel effect such as DICE, it is suggested that the parameters be systematically evaluated as outlined in Chapter 6.

# APPENDIX A

# DERIVATION OF SIMPLIFIED ENERGY-BALANCE EQUATION

The Appendix here concerns the derivation of the simplified form of the energy-balance equation (Eqn. (2.5)) which has been used as the basis for the non-local modeling of impact ionization as well as for velocity overshoot.

We first start from the semi-classical Boltzmann Transport Equation (BTE). It can be shown that by taking the first three moments of the BTE (the zeroth, the first, and the second) it is possible to obtain [Slo91]:

a. Carrier conservation (carrier continuity equation), the zeroth moment of the BTE;

b. Momentum conservation, the first moment of the BTE;

c. Energy conservation, the second moment of the BTE.

These three moments can be mathematically expressed as

$$\frac{\partial n}{\partial t} + \nabla \bullet (n\dot{v}) = G \quad , \tag{A.1}$$

$$\frac{\partial}{\partial t}\dot{p} + \dot{v} \bullet \nabla \dot{p} = (-q\dot{E}) - \frac{1}{n}\nabla(knT_e) - \frac{\dot{p}}{\tau_p} \quad , \tag{A.2}$$

$$\frac{\partial w}{\partial t} + \dot{v} \bullet \nabla w = -q\dot{E} \bullet \dot{v} - \frac{k}{n}\nabla \bullet nT_e\dot{v} - \frac{1}{n}\nabla \bullet \kappa \nabla T_e - \frac{w - w_0}{\tau_E} \quad , \tag{A.3}$$

where $G$ is the generation rate (for example due to impact ionization), $v$ is the velocity of the carriers, ***p*** is the carrier momentum, $\kappa$ is the electron thermal conductivity, *n* is the carrier concentration, w is the carrier energy expressed as $w = 1/2*m^*v^2 + 3/2*kT_e$, and $w_0$ is the equilibrium energy. The above equations have simple physical interpretations. Equation (A.1) is the carrier-conservation equation under transient conditions and in the presence of generation. Equation (A.2) is the carrier momentum-conservation equation. The left-hand side of (A.2) is the sum of the inertial and momentum outflow terms. The right-hand side of (A.2) is the gain in momentum due to an applied electric field and the force due to the electron pressure and the loss in momentum due to collisions (expressed simply as a relaxation term). Note that the second term in the right-hand side of (A.2) i.e., $nkT_e$, has units of pressure. This directly follows from the ideal gas law which states that $PV = NkT_e$ and hence, $P = nkT_e$, where N is total number of electrons in a given Volume (V) and n = N/V ($/cm^3$). Physically, this term represents a gradient in electron pressure which causes a net change in the carrier momentum and thus has to be accounted for in the momentum conservation equation. Equation (A.3) is the carrier energy-conservation equation. The left-hand side is the sum of the rate of change of energy and outflow terms. This must be equal to the energy rate supplied by the applied electric field, the work rate performed by the electron pressure, the divergence of the heat flow (or flux), and the rate of energy lost due to collisions.

## Derivation of Equation (2.5)

We start from (3), which is the energy conservation for electrons. Under steady-state conditions (d/dt =0), (A.3) reduces to

$$\dot{v} \bullet \nabla w = -q\dot{E} \bullet \dot{v} - \frac{k}{n}\nabla \bullet n T_e \dot{v} - \frac{1}{n}\nabla \bullet \kappa \nabla T_e - \frac{w - w_0}{\tau_E} \quad . \tag{A.4}$$

The heat flux $Q \equiv \kappa\nabla\ T_e$ is taken to be a constant, so that $\nabla.Q \approx 0$. Again, this approximation is strictly valid only where the temperature gradients are small. Expanding the second term in the right-hand side we get

$$\dot{v} \bullet \nabla w = -q\dot{E} \bullet \dot{v} - \frac{k}{n}(n\nabla \bullet (T_e \dot{v}) + (T_e \dot{v}) \bullet \nabla n) - \frac{w - w_0}{\tau_E} \quad . \tag{A.5}$$

Now, assuming that diffusion is negligible, we can ignore the term,$\nabla n/n$. In short-channel SOI MOSFETs under strong inversion, the current is predominantly due to drift. Therefore, this approximation may be justified. Now, (A.5) reduces to

$$\dot{v} \bullet \nabla w = -q\dot{E} \bullet \dot{v} - k(T_e \nabla \bullet \dot{v} + \dot{v} \bullet \nabla T_e) - \frac{w - w_0}{\tau_E}. \tag{A.6}$$

In the saturation region, the drift velocity is assumed to be constant and saturated ($v_{sat} \approx 10^7$ cm/s), and neglecting velocity overshoot (for the time being) we arrive at

$$\dot{v} \bullet \nabla w = -q\dot{E} \bullet \dot{v} - k(\dot{v} \bullet \nabla T_e) - \frac{w - w_0}{\tau_E} \quad . \tag{A.7}$$

The above equation is the required E-T relation for application in non-local impact ionization modeling. To use it in device/circuit simulators we can consider a 1-D n-channel MOSFET. By inspection we know the direction of the electric field, the velocity, and the temperature gradient. Using this information we can convert (A.7) into a scalar equation that can be solved for $T_e(y)$ given E(y). For an n-channel MOSFET, $\mathbf{E}(y).v(y) < 0$, $v(y).\nabla w > 0$, $v(y).\nabla T_e(y) > 0$. Therefore, we need to consider only the magnitude of the quantities once we use the appropriate sign in (A.7). Doing this yields

$$v\frac{dw}{dy} = q|E(y)|v - kv\frac{d}{dy}(T_e(y)) - \frac{w - w_0}{\tau_E} \quad . \tag{A.8}$$

Now using $w=3/2*k*T_e$ and $w_0=3/2*k*T_0$ in the above equation and simplifying yields,

$$\frac{d}{dy}(T_e - T_0) + \frac{(T_e - T_0)}{\lambda_E} = \frac{2q|E(y)|}{5k} \quad . \tag{A.9}$$

The above equation is the simplified form of energy-balance equation, (2.5).

# APPENDIX B

# WEAK-INVERSION FIELD CHARACTERIZATION FOR FD/ AND PD/SOI MOSFETs

This appendix concerns derivation of the field in weak inversion used for calculating (M-1) in Chapter 3. We first consider the weak-inversion field in the FD/SOI MOSFET.

## Field for the FD/SOI MOSFET

To characterize the field in weak inversion we apply Gauss's law to a pill box, ABCD, in the high-field region of the SOI MOSFET [Vee88]. This yields,

$$-\int_0^{t_b} \varepsilon_s(\Delta E_y(y))dx + \int_0^{t_b} \varepsilon_s(\Delta E_y(y+dy))dx + (\varepsilon_s \Delta E_{sb} - \varepsilon_s \Delta E_{sf})\Delta y = 0 \qquad \text{(B.1)}$$

(B.1) can be simplified using (B.2) and (B.3) shown below:

$$\Delta E_y(y+dy) - \Delta E_y(y) = \left(\frac{d}{dy}\Delta E_y\right)\Delta y = \frac{d^2}{dy^2}\Delta\psi(x, y) \quad , \qquad \text{(B.2)}$$

$$\frac{d^2}{dy^2}\int_0^{t_b} \Delta\psi(x, y) \cong \frac{1}{2}(\Delta\psi_{sf}(y) + \Delta\psi_{sb}(y)) \quad . \qquad \text{(B.3)}$$

Note that (B.3) is simply an approximation for the integral described in [Vee88]. Now using (B.2) and (B.3) in (B.1), and applying Gauss's law at the interface, we obtain:

$$\frac{\varepsilon_s t_b}{2}\frac{d^2}{dy^2}(\Delta\psi_{sf} + \Delta\psi_{sb}) = -\Delta Q_{cf} - \Delta Q_{cb} + C_{of}\Delta\psi_{sf} + C_{ob}\Delta\psi_{sb} \qquad \text{(B.4)}$$

In weak inversion, we can typically neglect the first two terms in the right hand side of the above equation [Gre93]. Also, for the FD/SOI MOSFET $\Delta\psi_{sf} \approx \Delta\psi_{sb}$ since the bands at the front and back are not pinned in weak inversion and hence tend to track each other. Using these assumptions yields the following (second order) differential equation in $\Delta\psi_{sf}$:

$$\frac{d^2}{dy^2}(\Delta\psi_{sf}) = \frac{\Delta\psi_{sf}}{l_{cf}^2} \quad , \qquad \text{(B.5)}$$

where $l_{cf}$ is a characteristic length in weak inversion given by $t_b(C_b/(C_{of}+C_{ob}))^{1/2}$. Applying the boundary conditions, $\Delta E_y(L_{ef}) \approx 0$ (current is due to only diffusion at $y = L_e$) and that $\Delta\psi_{sf}(L_{ef}) = \eta l_c^2$ gives and solving (B.5) gives,

$$|E_f(y)| \cong |E_b(y)| \cong \frac{\eta l_c^2}{l_{cf}} \sinh\left(\frac{y - L_e}{l_{cf}}\right) \quad . \qquad \text{(B.6)}$$

Note that $l_c$ and $l_{cf}$ are not the same. The corresponding channel length modulation at the front and back surfaces can be obtained by integrating (B.6) between 0 and $\Delta L$ (and setting the integral to $V_{DS}$). This gives,

$$\Delta L^{Wk} \equiv L - L_e = l_{cf} \ln\left(\frac{L^2}{l_c^2}\right) \qquad \text{(B.7)}$$

(B.6) and (B.7) are the required equations for the field for weak inversion impact ionization calculations for the FD/SOI MOSFET in Section 3.3.2. We now calculate the field in weak inversion for the PD/SOI MOSFET.

## Field Calculation for the PD/SOI MOSFET

The key differences in the analysis for the PD/SOI MOSFET are the assumptions used to simplify (B.4). In the PD/SOI MOSFET the back surface potential is pinned [Suh95], so that $\Delta\psi_{sb} \approx 0$. Now, applying Gauss's law at the front surface, yields

$$\varepsilon_{ox}E_{sf}(y) \cong -C_{of}\Delta\psi_{sf}(y) \tag{B.8}$$

Now, to evaluate $\Delta E_{sb}(y)$, we use the DIBL approximation [Suh95]. This gives,

$$\Delta E_{sb}(y) \cong \frac{\Delta\psi_{sf}(y)}{t_b} + \frac{\eta t_b}{2} \tag{B.9}$$

Using (B.8) and (B.9) in (B4) gives,

$$\frac{d^2}{dy^2}(\Delta\psi_{sf}) = \frac{\Delta\psi_{sf}}{l_c^2} + \eta \tag{B.10}$$

Solving (B.10) with similar boundary conditions to that applied for the FD/SOI MOSFET in weak inversion, i.e., $\Delta E_y(L_{ef}) \approx 0$ and that $\Delta\psi_{sf}(L_{ef}) = \eta l_c^2$ gives,

$$|E_f(y)| \cong 2\eta l_c \sinh\left(\frac{y - L_e}{l_c}\right) \quad . \tag{B.11}$$

The corresponding channel-length modulation at the front surface is given by,

$$\Delta L^{Wk} \equiv L - L_e = l_c \ln\left(\frac{L^2}{2l_c^2}\right) \tag{B.12}$$

(B.11) and (B.12) are the required equations for the field for weak inversion impact ionization calculations for the PD/SOI MOSFET in Section 3.3.3.

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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Jerry G. Fossum, Chairman
Professor of Electrical and Computer Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Sheng S. Li
Professor of Electrical and Computer Engineering

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Robert M Fox

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I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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